

# MX•COM, INC. MiXed Signal ICs

## APPLICATION NOTE

### MX909A Signal Acquisition Principles

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## Introduction

This Application Information publication provides guidance on the correct way of using the automatic level and timing extraction sequences of the MX909A as triggered by the AQLEV and AQBC bits of the Command Register.

The techniques detailed should work in most radio systems but slightly different operation could lead to worthwhile improvements for specific cases. Experimentation will be necessary to evaluate the performance of the procedures in comparison with system requirements.

## Bit Clock Extraction and Receive Level Measurement Principles

The clock extraction circuits operate by storing on-chip a current best estimate of the bit timing of the received signal. These clock extraction circuits track the timing of the input signal by monitoring the data zero-crossings. They will eventually lose track of the timing if these do not occur for extended periods.

As data is received the device continually updates the current best estimate, unless the 'Hold' setting is selected in which case the estimate is frozen. The input signal can change the internal estimate at a speed related to the bandwidth set (PLLBW).

During acquisition the PLLBW is initially set to 'Wide' and the input signal can then rapidly alter the internal estimate. As the clock extraction circuits home-in on the received data timing the bandwidth is automatically switched to 'Medium' for 30 bits to reduce the amount of jitter and hence improve the BER performance; the setting is then changed to the residual value (as set by the Control Register, PLLBW bits).

The 'Hold' setting is intended to enable clock retention during short fades.

The upper and lower voltages of the input signal, after internal filtering, are stored on external capacitors connected to the DOC1 and DOC2 pins. These are used to generate levels inside the device to enable the detection of zero-crossings and to extract the received binary data. As data is received, the values stored on these capacitors are updated to track amplitude variations and drift, unless 'Hold' is selected in which case the voltages will decay slowly towards VBIAS.

During acquisition the two capacitors are rapidly charged toward the input voltage over 1-bit period (Clamp), the capacitor voltages then follow the input signal using Lossy Peak Detect to quickly establish the upper and lower levels. As the signal is acquired the mode automatically changes to the residual setting (as set by the Control Register, LEVRES bits). The 'Hold' setting is intended to enable level retention during short fades.

Note that to operate correctly in the 'Peak Averaging' mode it is required that bit timing has already been established.

The level extraction circuits require the voltages present during pairs of '1's' and '0's', i.e. the upper and lower values. If '00' and '11' sequences do not occur for periods greater than approximately 100 bits the levels stored will not accurately reflect those of the input wave.:

## Acquisition Operation

The acquisition sequences available to the user of the MX909A are intended for 2 types of system:

1. 'Mobitex' type systems with some form of carrier or signal detect facility.
2. Systems with no carrier or signal detect indication.

In both cases it is assumed that the incoming signal to be detected consists of a bit sync pattern (..11001100..) followed by a system synchronization pattern and that the device is set to raise an interrupt when this occurs (an SFS or SFH task has been set). The following techniques should lead to reliable detection and acquisition of the start of isolated data for most radio systems. (See note on ac coupling).

### 'Mobitex-Type' - Carrier Detect Indication Available

The device must lock-on to the incoming signal within the 16 bits of bit sync; to achieve this it is necessary to activate both AQBC and AQLEV acquisition sequences at or before the start of the bit sync, typically during a period of unmodulated carrier which precedes messages. In this case the AQBC and AQLEV automatic sequences can be used with the residual settings for the PLLBW = 'Medium' or 'Narrow' and LEVRES = 'Peak Averaging'. The BER will improve toward its steady value over a period of approximately 30 bits from the start of the bit-sync.

It is important that when the AQLEV acquisition sequence is started the voltage level of the input wave is within, or at worst just outside, the extremes of a '11110000' data pattern.

### No 'Carrier Detect' Available

Where no carrier or signal detect circuitry is available the device has to lock onto the incoming signal with little or no cue from the controlling device, this will of course mean that acquisition will take longer and that decoding errors are more likely.

The MX909A must track the incoming signal continuously for a data signal and the best settings to achieve this will be PLLBW = 'Wide' and LEVRES = 'Lossy Peak Detect'. To initiate this the AQBC and AQLEV bits would need to be set with the residual PLLBW = 'Medium' or 'Narrow' and LEVRES = 'Lossy Peak Detect' or 'Peak Averaging'.

When the synchronization pattern is successfully detected the PLLBW and LEVRES functions will automatically sequence to the residual setting.

Where the device is required to detect a signal in this way it is recommended that the bit sync sequence of repetitive '..0011..' bits is extended from 16 (Mobitex spec.) to  $\geq 64$  or that the pre-message unmodulated carrier period is extended. Also it may be found advantageous to lengthen the frame sync sequence to reduce the possibility of frame sync falsing.

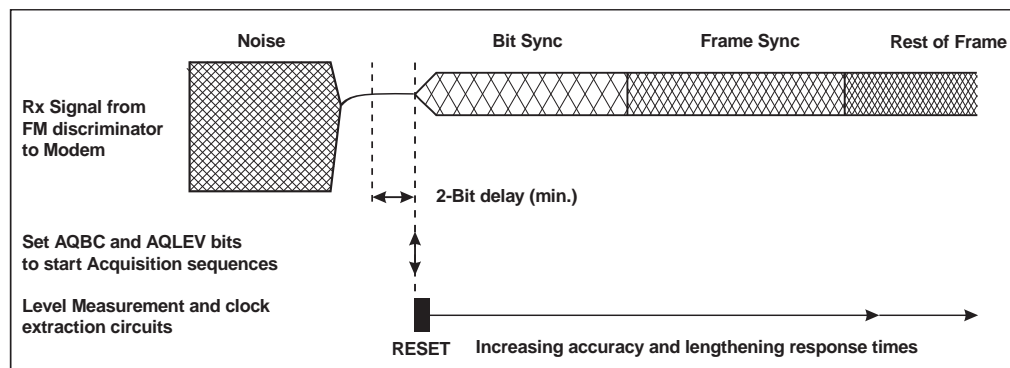


Figure 1: Bit Clock and Level Acquisition Example

## Acquisition Notes

### Frame Sync Falsing

When noise or an unmodulated carrier is fed into the device the output of the internal bit decode circuits will effectively be random data. This will have the effect of triggering the frame-sync detect circuit whenever this random data matches the frame-sync bytes programmed. There is little possibility of this happening if a Search for Frame Head or Search for Frame Sync task is set just before the beginning of the frame-sync bytes.

However if the device is set to detect a message a long time before it appears, and no carrier detect is available, the possibility of falsing is increased. This problem is aggravated in the case of the Mobitex system which specifies that the frame sync must be detected with up to any one bit in error; this raises the probability of falsing, due to random data, from 1 in  $2^{16}$  bits to 17 in  $2^{16}$  bits.

The user can significantly reduce the chances of falsing by providing extra frame sync bits after those programmed in the MX909A. For example, when receiving a signal with 4 bytes of frame sync the receiving device is programmed with the first two bytes (LFSB), when these are detected using the SFS task, two RSB tasks are issued.

Decoding of the signal only continues if these next 2 bytes match the last two bytes of the 4 byte frame sync otherwise the search would be restarted.

### Short Unmodulated Carrier and Bit Sync Sequences

The most critical case to be met is to use the MX909A in a system where no carrier detect or signal presence indicator is available, the frame-sync is short and the unmodulated carrier is present for a short period.

The device is required to lock-on to the incoming signal within 16 bits whilst also dealing with the potentially large dc and level changes that can occur just before the message is received.

Operating to such a system may result in some proportion of received messages being missed due to frame sync falsing and missing the frame sync bytes due to decoding errors. It is therefore recommended that the MX909A is used in systems with a short unmodulated carrier and bit sync sequences, only if a carrier detect or similar indication is available.

### AC Coupling

The effect of ac coupling is to reduce the static BER performance for a given S/N ratio as it causes low frequencies to be attenuated and cause dc changes to appear as a decaying voltage superimposed upon the signal. A carrier, giving a dc shift, coming on near the start of a message will have the effect of confusing the level detection circuitry and hence cause errors in extracting data. It would be better to delay the message appearing until any dc shift had decayed thus improving the likelihood of correct acquisition. In either case the automatic acquisition sequences can be used.

### Automatic Acquisition Sequences

Sequences of operation for automatic acquisition. For situations when a bit sync pattern is not being searched for (SFS or SFH is not set) the MX909A uses a fixed number of bits delay in switching between the modes:

#### AQLEV

SFH or SFS is set within 28 bits of AQLEV being set:

- 1 bit of clamp
- Lossy peak detect until frame sync is detected
- Residual setting

SFH or SFS is not set: 1 bit of clamp

- 30 bits of Lossy peak detect
- Residual setting

#### AQBC

SFH or SFS is set within 14 bits of AQBC being set:

- 'Wide setting' until frame sync detected
- 30 bits of 'Medium setting'
- Residual setting

SFH or SFS is not set: 16 bits of 'Wide setting'

- 30 bits of 'Medium setting'
- Residual setting