CY2071A

Low-Cost Single-PLL Clock Generator

Features

- **General purpose clock synthesizer for all applications – such as modems, disk drives, CD-ROM drives, games, set-top boxes, data/telecommunications, etc.**
- **EPROM configurable for quick availability and prototyping.**
- **Three configurable clock outputs**
- **Outputs ranging from 500 kHz to 100 MHz (5V) and up to 80 MHz for 3.3V operation**
- **Phase-locked loop oscillator input derived from external crystal (10 MHz to 25 MHz) or external reference clock (1 MHz to 32 MHz)**
- **3.3V or 5V operation (configurable)**
- **8-pin 150-mil packaging achieves minimum footprint for space-critical applications**
- **Sophisticated internal loop filter requires no external components or manufacturing tweaks as commonly required with external filters**

Functional Description

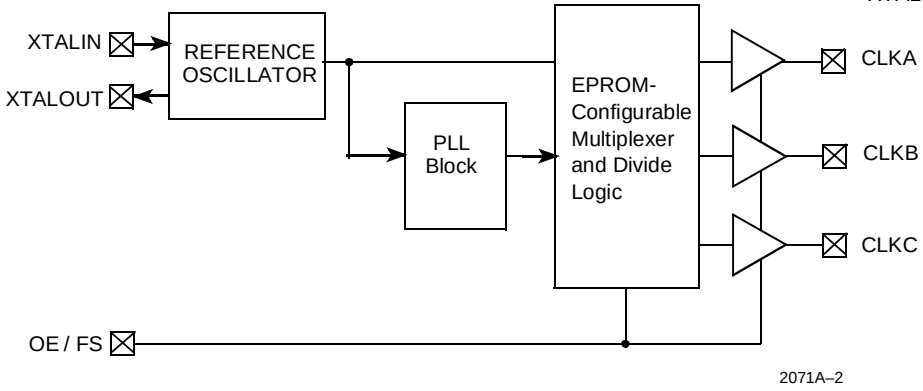
The CY2071A is a general-purpose clock synthesizer designed for use in applications such as modems, disk drives, CD-ROM drives, video CD players, games, set-top boxes and data/telecommunications. The device offers up to three configurable clock outputs in an 8-pin 150-mil SOIC package and can operate off either a 3.3V or 5V power supply. The on-chip reference oscillator is designed for 10 MHz to 25 MHz crystals. Alternatively, an external reference clock of frequency between 1 MHz and 32 MHz can be used.

The CY2071A has one PLL and outputs three factory-EPROM configurable clocks: CLKA, CLKB, and CLKC. The output clocks can originate either from the PLL or the reference, or selected dividers thereof. Additionally, pin 8 can be configured to be an Output Enable or a Select input. The latter facilitates two independent frequencies on all outputs driven by the same PLL. Please see the configuration form located at the back of this datasheet for more details.

The CY2071A can replace multiple Metal Can Oscillators (MCO) in a synchronous system, providing cost and board space savings to the manufacturer. Hence, these devices are ideally suited for applications that require multiple, accurate, and stable clocks synthesized from low-cost generators in small packages. A hard disk drive is an example of such an application. In this case, CLKA drives the PLL in the Read Controller, while CLKB and CLKC drive the MCU and associated sequencers.

Consider using the CY2081 for applications that require unrelated output frequencies. Consider using the CY2291, CY2292, or CY2907 for applications that require more than three output clocks.

Logic Block Diagram



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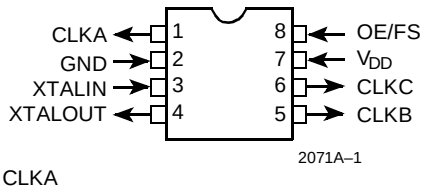
Pin Configuration

SOIC
Top View



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Pin Summary

Name	Number	Description
CLKA	1	Configurable clock output
GND	2	Ground
XTALIN[1]	3	Reference Crystal Input or External Reference Clock Input
XTALOUT[1, 2]	4	Reference Crystal Feedback
CLKB	5	Configurable clock output
CLKC	6	Configurable clock output
V_{DD}	7	Voltage Supply
OE / FS	8	Output Control Pin, either Output Enable or Frequency Select input. (Active-HIGH, internal pull-up resistor to V_{DD})

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage ..... –0.5V to +7.0V

DC Input Voltage..... –0.5V to V_{DD}+0.5V

Storage Temperature ..... –65°C to +150°C

Max. Soldering Temperature (10 sec) .....260°C

Junction Temperature.....150°C

Static Discharge Voltage ..... >2000V (per MIL-STD-883, Method 3015)

Operating Conditions[3]

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage	4.5 (3.0)	5.5 (3.6)	V
T_A	Operating Temperature, Ambient	0	70	°C
C_L	Max. Load Capacitance per output		25 (15)	pF
f_{REF}	External Reference Crystal	10.0	25.0	MHz
f_{REF}	External Reference Clock[4, 5]	1.0	32.0	MHz

Electrical Characteristics V_{DD} = 5V (3.3V) ±10%, T_A = 0°C to +70°C

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{OH}	HIGH-Level Output Voltage	I_{OH} = –4.0 mA	2.4			V
V_{OL}	LOW-Level Output Voltage	I_{OL} = 4.0 mA			0.4	V
V_{IH}	HIGH-Level Input Voltage[6]	Except Crystal Pins	2.0			V
V_{IL}	LOW-Level Output Voltage[6]	Except Crystal Pins			0.8	V
I_{IH}	Input HIGH Current	V_{IN} = V_{DD} – 0.5V			10	µA
I_{IL}	Input LOW Current	V_{IN} = 0.5V			150	µA
I_{OZ}	Output Leakage Current	Three State Outputs			250	µA
I_{DD}	V_{DD} Supply Current[7]	V_{DD} = V_{DD} max. 5V (3.3V) operation, C_L = 25 pF (15 pF)		40 (24)	60 (40)	mA

Notes:

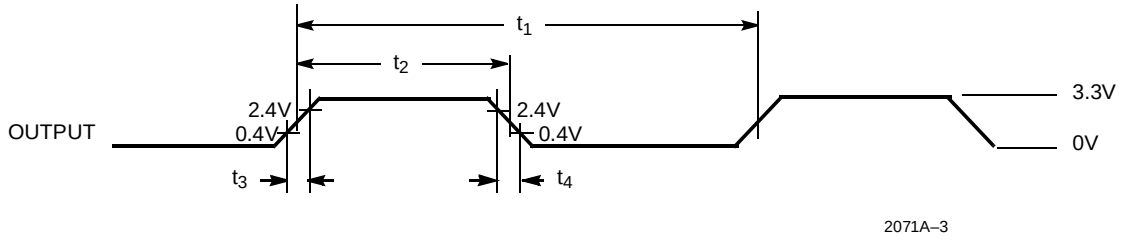
1. For best accuracy, use a parallel-resonant crystal, C_L=17 pF.
2. Float XTALOUT pin if XTALIN is driven by reference clock (as opposed to an external crystal).
3. Electrical parameters are guaranteed with these operating conditions. Values for 3.3V operation are shown in parentheses.
4. External input reference clock must have a duty cycle between 40% and 60%, measured at V_{DD}/2.
5. Please refer to application note “Crystal Oscillator Topics” for information on AC-coupling the external input reference clock.
6. Xtal inputs have CMOS thresholds.
7. Load = max, typical configuration, f_{REF} = 14.318 MHz. Specific configurations may vary. A close approximation of I_{DD} can be derived by the following formula: $I_{DD}(mA) = V_{DD}*(6.25+(0.055*F_{REF}) + (0.0017*C_{LOAD}*(F_{CLKA}+F_{CLKB}+F_{CLKC})))$. C_{LOAD} is specified in pF and F is specified in MHz.

Switching Characteristics[8]

Parameter	Name	Description	Min.	Typ.	Max.	Unit
t_1	Output Period	Clock output range, 5V operation	10 [100 MHz]		2000 [500 KHz]	ns
t_1	Output Period	Clock output range, 3.3V operation	12.5 [80 MHz]		2000 [500 KHz]	ns
t_{1A}	Clock Jitter	Peak-to-peak period jitter (t_1 max. – t_1 min.), % of clock period, $f_{OUT} \leq 16$ MHz		0.8	1	%
t_{1B}	Clock Jitter	Peak-to-peak period jitter (16 MHz ≤ f_{OUT} ≤ 50 MHz)		350	500	ps
t_{1C}	Clock Jitter	Peak-to-peak period jitter ($f_{OUT} \geq 50$ MHz)		250	350	ps
	Output Duty Cycle	Duty cycle[9,10] for outputs, ($t_2 \div t_1$), C_L = 25 pF (15 pF at 3.3V), $f_{OUT} \leq 60$ MHz	45%	50%	55%	
	Output Duty Cycle	Duty cycle[10] for outputs, ($t_2 \div t_1$), C_L = 25 pF (15 pF at 3.3V), $f_{OUT} \geq 60$ MHz	40%	50%	60%	
t_3	Rise time	Output clock rise time at C_L = 25 pF (15 pF at 3.3V operation)		1.5	2.5	ns
t_4	Fall time	Output clock fall time at C_L = 25 pF (15 pF at 3.3V operation)		1.5	2.5	ns

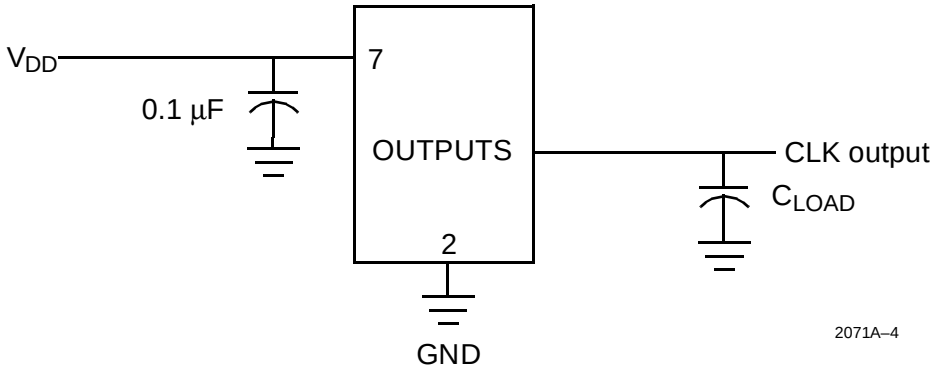
Switching Waveforms

All Outputs Duty Cycle and Rise/Fall Time



Notes:
8. Guaranteed by design, not 100% tested.
9. Reference Output duty cycle depends on XTALIN duty cycle .
10. Measured at 1.4V.

Test Circuit



Ordering Information

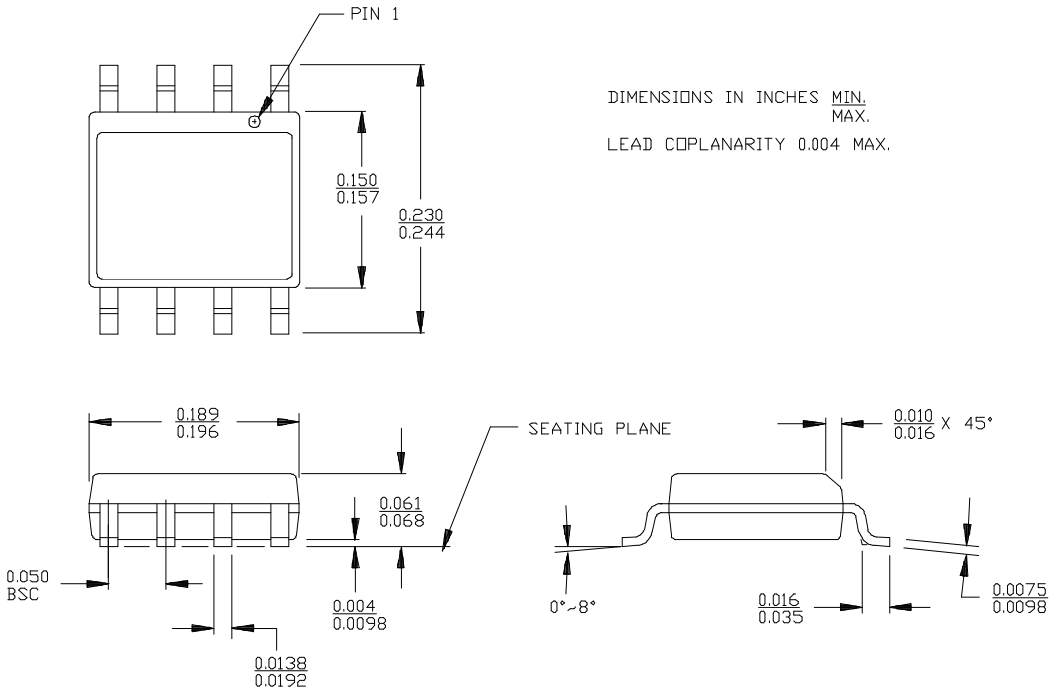
Ordering Code	Package Name	Package Type	Operating Range
CY2071ASC–XXX	S8	8-Pin (150-Mil) SOIC	5.0V, Commercial[11]
CY2071ASL–XXX	S8	8-Pin (150-Mil) SOIC	3.3V, Commercial[11]

Notes:
11. 0°C to +70°C

Document #: 38–00521

Package Diagram

8-Lead (150-Mil) SOIC S8



CY2071A CONFIGURATION REQUEST FORM

Customer _____ Engineer _____ FAE/Sales _____

Phone # _____ Fax # _____ Date _____

1. OPERATING VOLTAGE (circle one) 3.3V 5.0V

2. INPUT REFERENCE FREQUENCY (Circle one) Crystal External Clock

Default reference= 14.318 MHz. If a different reference is desired, Specify the frequency in the box to the right (must be between 10 MHz and 25 MHz for crystal, 1 MHz and 32 MHz for external clock):

Actual Input Frequency (MHz): _____

3. OUTPUT CONTROL PIN (PIN 8) CONFIGURATION (Circle One) OE FS

4. PLL FREQUENCY

	Requested	Actual
FS = 0		
FS = 1		

← Request only if pin 8 is configured to be a FS input

Range: 2–100 MHz at 5V; 2–80 MHz at 3.3V

5. OUTPUT CONFIGURATION

Use the table below to select your output configuration. Write in the option number and output frequency in the boxes provided. Output frequencies must fall within the range specified in the datasheet. After completing this form, please fax it to your local Cypress representative.

Output Options Table

1.PLL	2.PLL/2	3.PLL/3	4.PLL/4	5.PLL/5
6.PLL/8	7.REF	8.REF/2	9.OFF	

	Option	Frequency
CLKA		
CLKB		
CLKC		

Notes:

- Buffered reference clock is available on any output
- Outputs can range from 500 kHz to 100 MHz (80 MHz at 3.3V)

6. FOR CYPRESS USE ONLY

Customer Configuration	Marking
Date	Quantity