CY2907

General Purpose Clock Synthesizer

Features

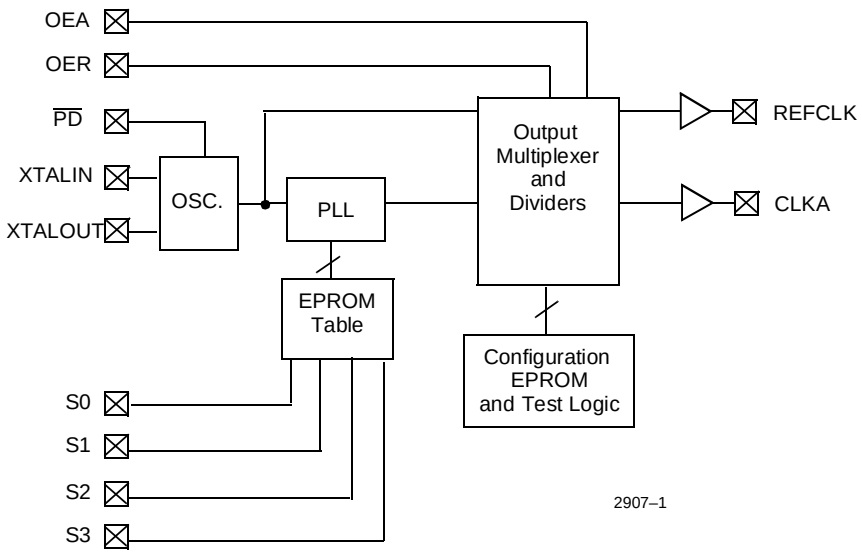
- **Highly configurable single PLL clock synthesizer provides all clocking requirements for numerous applications**
- **Compatible with all industry standard 9107 and 9108 pinouts.**
- **1 MHz to 32 MHz input reference frequency (depending on option)**
- **Up to 16 user-selectable output frequencies in one configuration**
- **Output frequencies from 2 MHz to 120 MHz at 5.0V (2 MHz to 90 MHz at 3.3V)**
  - **— Secondary output clock available (REFCLK) as a function of CLKA or as a buffered reference clock**
- **EPROM programmability for Quick-turn custom versions much faster than metal mask design change**
- **Power-down function available**
- **± 250ps absolute jitter**
- **Available in 8-pin or 14-pin SOIC packages**
- **3.3V or 5.0V operation**

Functional Description

The CY2907 is a general-purpose Clock Synthesizer/Driver chip. The CY2907 generates multiple system clocks at different frequencies from a single reference frequency input. The CY2907 can be used in a wide variety of applications — from graphics to PC motherboards to disk drives. Any application that requires more than one clock frequency can benefit from using the CY2907.

The CY2907 is configured with an EPROM array, making it easily customizable for any application. Custom versions of the CY2907 with user-defined features and frequencies are available. Refer to the custom configuration form at the back of this document and contact your local Cypress representative for more details. The CY2907 is compatible with all industry standard 9107 and 9108 clock synthesizers.

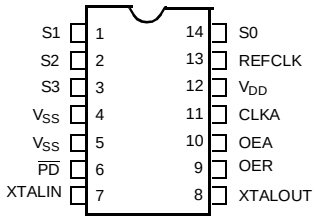
Logic Block Diagram



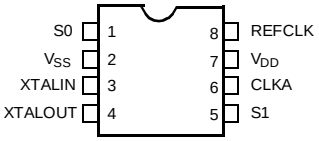
2907–1

Pin Configurations [1]

Top View
SOIC –03/–11



SOIC –05/–10



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Note:
1. Additional configurations available. Refer to the custom configuration form at the back of this document, and contact your local Cypress representative for more information.

Pin Summary

Name	Option: –03,–11 Pin Number	Option: –05,–10 Pin Number	Description
S1	1	5	Frequency select (CLKA) (Internal pull-up resistor to V_{DD})
S2	2		Frequency select (CLKA) (Internal pull-up resistor to V_{DD})
S3	3		Frequency select (CLKA) (Internal pull-up resistor to V_{DD})
V_{SS}	4	2	Ground
V_{SS}	5		Ground
PD	6		Power Down (active LOW) (Internal pull-up resistor to V_{DD})
XTALIN[2]	7	3	Reference crystal input
XTALOUT[2,3]	8	4	Reference crystal feedback
OER	9		REFCLK Output enable (active HIGH) (Internal pull-up resistor to V_{DD})
OEA	10		CLKA Output enable (active HIGH) (Internal pull-up resistor to V_{DD})
CLKA	11	6	Clock output
V_{DD}	12	7	Voltage supply
REFCLK	13	8	Reference clock output
S0	14	1	Frequency select (CLKA) (Internal pull-up resistor to V_{DD})

Select Pin Definitions[1]

Option				–03[4]	–11
Input Frequency (MHz)				14.318	14.318
Select Pins:				Output Frequency (MHz):	
S3	S2	S1	S0	CLKA	CLKA
0	0	0	0	16.00	16.00
0	0	0	1	39.99	33.39
0	0	1	0	50.11	50.11
0	0	1	1	80.01	80.01
0	1	0	0	66.58	66.58
0	1	0	1	100.23	100.23
0	1	1	0	8.02	60.00
0	1	1	1	4.01	4.01
1	0	0	0	8.02	8.02
1	0	0	1	20.00	20.05
1	0	1	0	25.06	25.06
1	0	1	1	40.01	39.99
1	1	0	0	33.29	33.25
1	1	0	1	50.11	50.11
1	1	1	0	4.01	30.00
1	1	1	1	2.05	4.01

Option		–05	–10
Input Frequency (MHz)		14.318	14.318
Select Pins:		Output Frequency (MHz):	
S1	S0	CLKA	CLKA
0	0	40.01	25.057
0	1	50.11	33.289
1	0	66.61	40.006
1	1	80.01	50.113

Notes:

2. For best accuracy, use a parallel-resonant crystal, $C_{LOAD} \approx 17$ pF.
3. Float XTALOUT pin if XTALIN is driven by reference clock (as opposed to crystal).
4. CY2907-3 has smooth frequency transitions between any of the two groups of eight frequencies (S3 = 0 or S3 = 1), so that the device will switch glitch-free between 4-100 MHz and 2-50 MHz.

Maximum Ratings

(Beyond which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage .....–0.5 to +7.0V

Input Voltage .....–0.5V to V_{DD}+0.5V

Storage Temperature (Non-Condensing) ... –65°C to +150°C

Max. Soldering Temperature (10 sec) ..... +260°C

Junction Temperature ..... +150°C

Static Discharge Voltage ..... >2000V (per MIL-STD-883, Method 3015)

Operating Conditions[5]

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage, 5V Operation	4.5	5.5	V
V_{DD}	Supply Voltage, 3.3V Operation	3.0	3.7	V
T_A	Operating Temperature, Ambient	0	70	°C
C_L	Max. Capacitive Load		15	pF

Electrical Characteristics at 5.0V V_{DD} = 4.5V to 5.5V, T_A = 0°C to +70°C

Parameter	Description	Test Conditions			Min.	Max.	Unit
V_{IH}	High-level Input Voltage	Except Crystal Inputs			2.0		V
V_{IL}	Low-level Input Voltage	Except Crystal Inputs				0.8	V
V_{OH}[6]	High-level Output Voltage	V_{DD} = V_{DD} Min.	I_{OH} = –30 mA	CLKA	2.4		V
V_{OL}[6]	Low-level Output Voltage	V_{DD} = V_{DD} Min.	I_{OL} = 10 mA	CLKA		0.4	V
I_{OH}[6]	Output High Current	V_{OH} = 2.0V				–35	mA
I_{OL}[6]	Output Low Current	V_{OL} = 0.8V			22		mA
I_{IH}	Input High Current	V_{IH} = V_{DD}			–2	2	µA
I_{IL}	Input Low Current	V_{IL} = 0V				20	µA
I_{DD}[7]	Power Supply Current	$\overline{PD}$ HIGH, 50 MHz				42	mA
I_{DD}	Power Supply Current	$\overline{PD}$ LOW, Logic Inputs LOW				100	µA
I_{DD}	Power Supply Current	$\overline{PD}$ LOW, Logic Inputs HIGH				40	µA
R_{PU}[6]	Pull-up resistor	V_{IN} = V_{DD} – 1.0 V				700	kΩ

Electrical Characteristics at 3.3V V_{DD} = 3.0V to 3.7V, T_A = 0°C to +70°C

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{IH}	High-level Input Voltage	Except Crystal Inputs	0.7*V_{DD}		V
V_{IL}	Low-level Input Voltage	Except Crystal Inputs		0.2*V_{DD}	V
V_{OH}[6]	High-level Output Voltage	CLKA, I_{OH} = –5 mA	0.85*V_{DD}		V
V_{OL}[6]	Low-level Output Voltage	CLKA, I_{OL} = 6 mA		0.1*V_{DD}	V
I_{OH}[6]	Output High Current	V_{OH} = 0.7*V_{DD}		–10	mA
I_{OL}[6]	Output Low Current	V_{OL} = 0.2*V_{DD}	15		mA
I_{IH}	Input High Current	V_{IH} = V_{DD}	–2	2	µA
I_{IL}	Input Low Current	V_{IL} = 0V		10	µA
I_{DD}[7]	Power Supply Current	$\overline{PD}$ HIGH, CLKA = 50 MHz		40	mA
I_{DD}	Power Supply Current	$\overline{PD}$ LOW, Logic Inputs LOW		40	µA
I_{DD}	Power Supply Current	$\overline{PD}$ LOW, Logic Inputs HIGH		12	µA
R_{PU}[6]	Pull-up resistor	V_{IN} = V_{DD} – 0.5V		900	kΩ

Notes:

5. Electrical parameters are guaranteed with these operating conditions.
6. Guaranteed by design, not 100% tested in production
7. Load = max. typical configuration, f_{REF} = 14.318 MHz. Specific configurations may vary. A close approximation of I_{DD} can be derived by the following formula: I_{DD} (mA) = V_{DD} * (6.25 + (0.055*F_{REF}) + (0.0017*C_{LOAD}*(F_{CLKA} + REFCLK))). C_{LOAD} is specified in pF and F is specified in MHz.

Switching Characteristics at 5.0V [6]

Parameter	Output	Description	Test Conditions	Min.	Max.	Unit
t_R	CLKA	Output Rise Time 0.8V to 2.0V	15 pF Load		1.40	ns
t_F	CLKA	Output Fall Time 2.0V to 0.8V	15 pF Load		1.00	ns
t_R	CLKA	Output Rise Time 20% to 80%	15 pF Load		3.5	ns
t_F	CLKA	Output Fall Time 80% to 20%	15 pF Load		2.5	ns
t_D	CLKA	Duty Cycle	15 pF Load at 1.4V	45.0	55.0	%
F_I	XTALIN	Input Frequency	Crystal Oscillator	10	25	MHz
F_I	XTALIN	Input Frequency	External Input Clock[6]	1	32	MHz
F_O	CLKA	Output Frequency		2.0	120.0	MHz
t_{JIS}	CLKA	Jitter (One Sigma)	20 MHz to 100 MHz		150	ps
t_{JIS}	CLKA	Jitter (One Sigma)	14 MHz to 20 MHz		200	ps
t_{JIS}	CLKA	Jitter (One Sigma)	Less than 14 MHz		1	%
t_{JAB}	CLKA	Jitter (Absolute)	20 MHz to 100 MHz	– 250	+ 250	ps
t_{JAB}	CLKA	Jitter (Absolute)	14 MHz to 20 MHz	– 500	+ 500	ps
t_{JAB}	CLKA	Jitter (Absolute)	Less than 14 MHz		3	%
t_{PU}		Power-up Time			18	ms
t_{FT}	CLKA	Transition Time	8 MHz to 66.6 MHz		13	ms

Switching Characteristics at 3.3V [6]

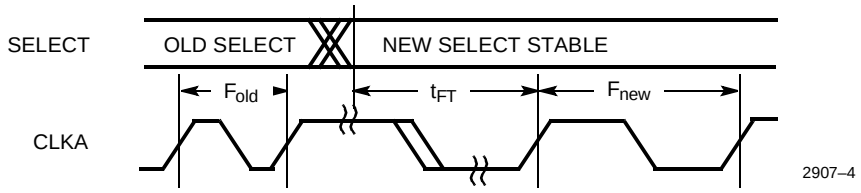
Parameter	Output	Description	Test Conditions	Min.	Max.	Unit
t_R	CLKA	Output Rise Time 20% to 80%	15 pF Load		3.5	ns
t_F	CLKA	Output Fall Time 80% to 20%	15 pF Load		2.5	ns
t_D	CLKA	Duty Cycle	15 pF Load at 1.4V	40.0	53.0	%
F_I	XTALIN	Input Frequency	Crystal Oscillator	10	25	MHz
F_I	XTALIN	Input Frequency	External Input Clock[8]	1	32	MHz
F_O	CLKA	Output Frequency		2.0	90.0	MHz
t_{JIS}	CLKA	Jitter (One Sigma)	25 MHz to 85 MHz		150	ps
t_{JIS}	CLKA	Jitter (One Sigma)	14 MHz to 25 MHz		200	ps
t_{JIS}	CLKA	Jitter (One Sigma)	Less than 14 MHz		1	%
t_{JAB}	CLKA	Jitter (Absolute)	25 MHz to 85 MHz	–250	+250	ps
t_{JAB}	CLKA	Jitter (Absolute)	14 MHz to 25 MHz	–500	+500	ps
t_{JAB}	CLKA	Jitter (Absolute)	Less than 14 MHz		3	%
t_{PU}		Power-up Time			18	ms
t_{FT}	CLKA	Transition Time	8 MHz to 66.6 MHz		13	ms

Notes:

8. Please refer to the application note “Crystal Oscillator Topics” when using an external reference clock as an input frequency source.

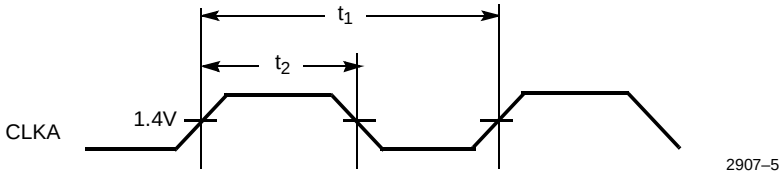
Switching Waveforms

Frequency Select Change (Transition Time)

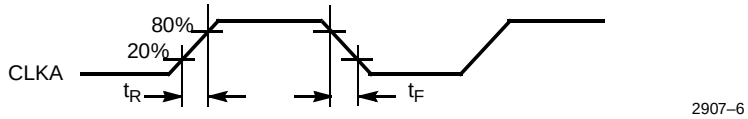


Duty Cycle Timing

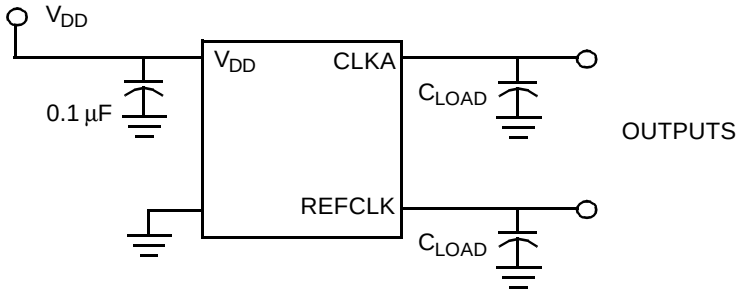
$t_D = t_2 \div t_1$



All Outputs Rise/Fall Time



Test Circuit



Note: All capacitors should be placed as close to each pin as possible.

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY2907SC–xxx	S8, S14	8-pin or 14-pin SOIC	Commercial

Document #: 38–00505–A

CY2907 CUSTOM CONFIGURATION REQUEST FORM

Company _____ Engineer _____ FAE/Sales _____

Phone# _____ Fax# _____ Date _____

The CY2907 is a factory EPROM-programmable single PLL clock synthesizer. The CY2907 can be configured to support the clocking needs of many types of applications. In addition to the standard configurations described in the datasheet, custom configurations with user-defined frequencies and features can be obtained. Follow the steps outlined in this form contact your local Cypress representative to request your custom configuration of the CY2907.

1. **OPERATING VOLTAGE** (Circle one) **3.3V** **5.0V**

2. **DESIRED PACKAGE SIZE** (Circle one) **8-pin** **14-pin**
   Please note that all functions may not fit in the 8-pin package

3. **PACKAGE TYPE** (Circle one) **DIP** **SOIC**

4. **INPUT REFERENCE FREQUENCY** (Circle one) **Crystal** **External Clock** **14.318 MHz** (Default)
   If a different reference is required, specify the frequency in the box to the right
   (must be between 10 MHz and 25 MHz for crystal, 1 MHz and 32 MHz for external clock): _____

5. **PLL FREQUENCIES** Complete the appropriate table for either 8-pin or 14-pin option.

14-pin

Select (S3..S0)	Requested	Actual
0000		
0001		
0010		
0011		
0100		
0101		
0110		
0111		
1000		
1001		
1010		
1011		
1100		
1101		
1110		
1111		

Range: 2– 120 MHz at 5V; 2– 90 MHz at 3.3V

8-pin

Select (S1..S0)	Requested	Actual
0 0		
0 1		
1 0		
1 1		

Range: 2– 120 MHz at 5V; 2– 90 MHz at 3.3V

6. **OUTPUT CONFIGURATION**
   Use the table below to select up to two outputs. Write in the number of the output in the boxes provided.
   Actual output frequencies must fall within the range of Output Frequency, F_O, described in the datasheet.

Output Options Table

1.PLL	2. PLL/2	3. PLL/3	4. PLL/4	5. PLL/5
6. PLL/8	7. Ref	8. Ref/2	9. Off	

CLKA OUTPUT _____ **REFCLK OUTPUT** _____

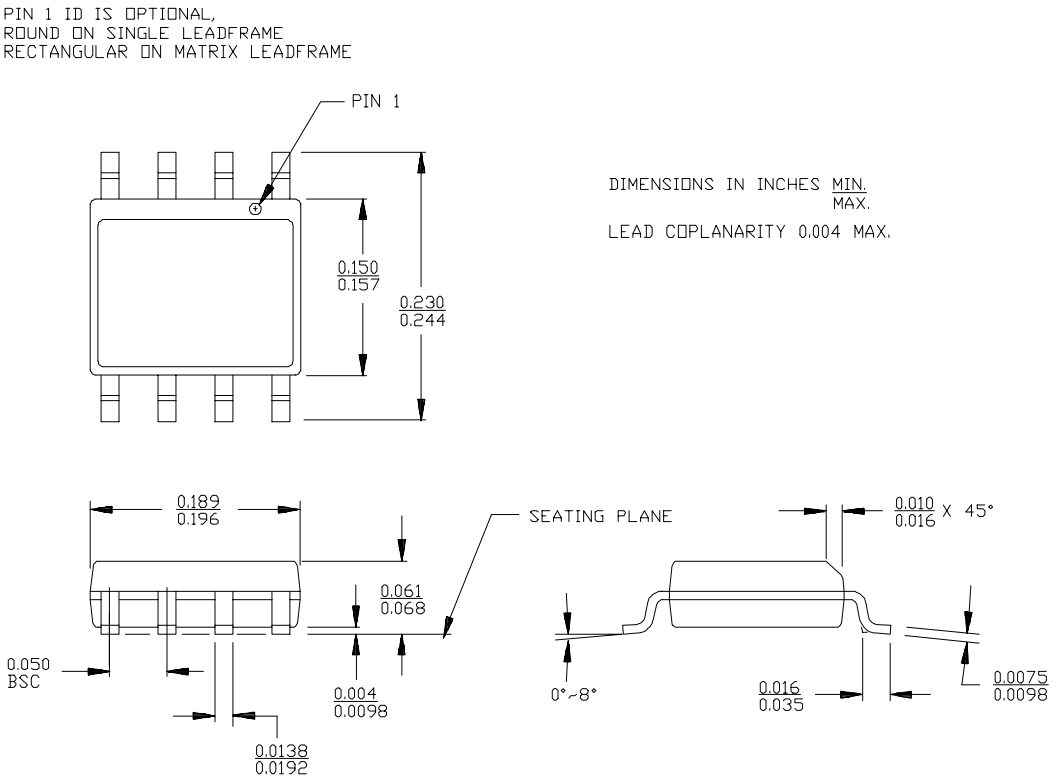
This form can be configured using CyClocks™ software which is available from the Cypress Website (http://www.cypress.com), or your local Cypress representative.

FOR CYPRESS USE ONLY (Shaded areas above and below)

Customer Configuration	Marking
Date	Quantity

Package Diagram

8-Lead (150-Mil) SOIC S8



14-Lead SOIC S14