HARRIS SEMICONDUCTOR

HFA3926

ADVANCE INFORMATION

February 1997

2.0GHz - 2.7GHz 250mW Power Amplifier

Features

- **Highly Integrated Power Amplifier with T/R Switch**
- **Operates Over 2.7V to 6V Supply Voltage**
- **High Linear Output Power (P_{1dB}: +24.5dBm)**
- **Low Cost SSOP-28 Plastic Package**

Applications

- **Wireless Local Loop Systems**
- **Systems Targeting IEEE 802.11 Standard**
- **TDD Quadrature-Modulated Communication Systems**
- **Wireless Local Area Networks**
- **PCMCIA Wireless Transceivers**
- **ISM Systems**

PRISM™

Description

The Harris HFA3926 is an integrated power amplifier with transmit/receive switch in a low cost SSOP 28 plastic package. The power amplifier delivers +27dB of gain with high efficiency and can be operated with voltages as low as 2.7V. The power amplifier switch is fully monolithic and can be controlled with CMOS logic levels.

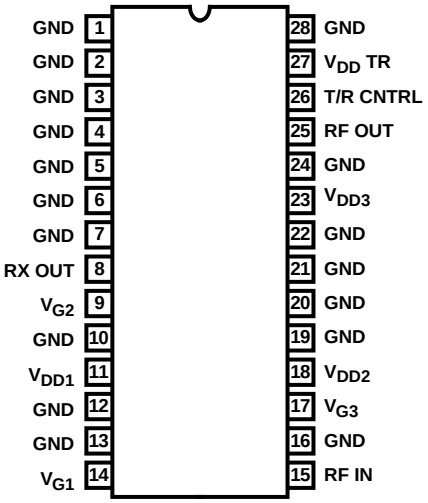
The HFA3926 is ideally suited for QPSK, BPSK or other linearly modulated systems in the 2.4GHz Industrial, Scientific, and Medical (ISM) frequency band. It can also be used in GFSK systems where levels of +25dBm are required. Typical applications include Wireless Local Area Network (WLAN) and Wireless Local Loop systems.

Ordering Information

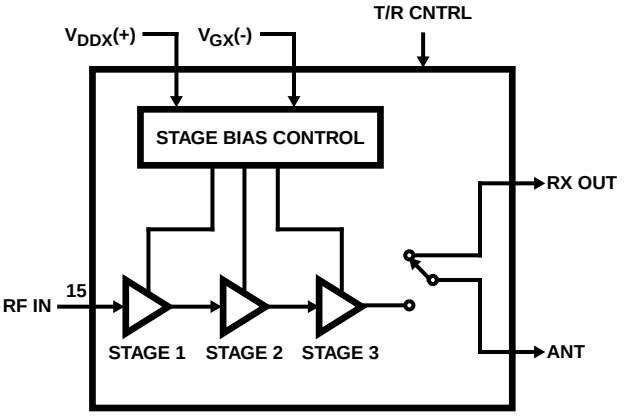
PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
HFA3926IA	-40 to 85	28 Ld SSOP	M28.15
HFA3926IA96	-40 to 85	Tape and Reel	

Pinout

HFA3926
(SSOP)
TOP VIEW



Functional Block Diagram



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CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **4282**

Pin Description

PINS	SYMBOL	DESCRIPTION
1	GND	DC and RF Ground.
2	GND	DC and RF Ground.
3	GND	DC and RF Ground.
4	GND	DC and RF Ground.
5	GND	DC and RF Ground.
6	GND	DC and RF Ground.
7	GND	DC and RF Ground.
8	RX OUT	Output of T/R Switch for receive mode.
9	V_{G2}	Negative bias control for the second PA stage, adjusted to set V_{DD2} quiescent bias current, which is typically 70mA. Typical voltage at pin = -0.55V. Input impedance: > 1MΩ.
10	GND	DC and RF Ground.
11	V_{DD1}	Positive bias for the first stage of the PA, 2.7V to 6V.
12	GND	DC and RF Ground.
13	GND	DC and RF Ground.
14	V_{G1}	Negative bias control for the first PA stage, adjusted to set V_{DD1} quiescent bias current, which is typically 20mA. Typical voltage at pin = -0.75V. Input impedance: > 1MΩ.
15	RF IN	RF Input of the Power Amplifier.
16	GND	DC and RF Ground.
17	V_{G3}	Negative bias control for the third PA stage, adjusted to set V_{DD3} quiescent bias current, which is typically 90mA. Typical voltage at pin = -0.95V. Input impedance: > 1MΩ.
18	V_{DD2}	Positive bias for the second stage of the PA. 2.7V to 6V.
19-22	GND	DC and RF Ground.
23	V_{DD3}	Positive bias for the third stage of the PA. 2.7V to 6V.
24	GND	DC and RF Ground.
25	RF OUT	RF output of T/R switch and power amplifier for transmit mode.
26	T/R CTRL	0V for transmit mode, +5V for receive mode.
27	V_{DD} TR	V_{DD} for T/R switch.
28	GND	DC and RF Ground.

Absolute Maximum Ratings

Maximum Input Power (Note 1) . . . . . +23dBm
Operating Voltages (Notes 1, 2) . . . . . V_{DD} = 8V, V_{GG} = -8V

Thermal Information

Thermal Resistance (Typical, Note 3) θ_{JA} (^{o}C/W)
SSOP Package 88
Maximum Storage Temperature Range . . . . . -65^{o}C to 150^{o}C

Operating Conditions

Temperature Range . . . . . -40^{o}C to 85^{o}C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Ambient temperature (T_A) = 25^{o}C.
2. $|V_{DD}| + |V_{GG}|$ not to exceed 12V.
3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

T_A = 25^{o}C, Z_0 = 50Ω, V_{DD} = +5V, P_{IN} = -30dBm, f = 2.45GHz, Unless Otherwise Specified

PARAMETER	MIN	TYP	MAX	UNITS
POWER AMPLIFIER INPUT FREQUENCY RANGE				
Linear Gain				
2.0GHz - 2.5GHz	27	28	32	dB
2.5GHz - 2.7GHz	23.5	27	-	dB
VSWR In/Out	-	1.75:1	-	
Input Return Loss	-	-11.3	-	dB
Output Return Loss	-	-11.3	-	dB
Output Power at P_{1dB} 2.0GHz - 2.7GHz	23	24.5	-	dBm
Second Harmonic at P_{1dB}	-	-20	0	dBc
Third Harmonic at P_{1dB}	-	-30	-10	dBc
I_{DD} at P1dB (V_{DD1} + V_{DD2} + V_{DD3})	-	270	375	mA

Typical Performance Curves

Power Amplifier Small Signal Performance NOTE: All data measured at T_A = 25^{o}C and V_{G1}, V_{G2} and V_{G3} adjusted for first stage quiescent current of 20mA, second stage current of 50mA and third stage current of 90mA, respectively.

TBD

FIGURE 1. LINEAR GAIN

TBD

FIGURE 2. INPUT MATCH

Typical Performance Curves (Continued)

TBD

FIGURE 3. OUTPUT MATCH

Power Amplifier CW Performance at Various Supply Voltages NOTE: All data measured at $T_A = 25^oC$ and V_{G1}, V_{G2} and V_{G3} adjusted for first stage quiescent current of 20mA, second stage current of 50mA and third stage current of 90mA, respectively.

TBD

FIGURE 4. POWER OUTPUT

TBD

FIGURE 5. POWER ADDED EFFICIENCY

TBD

FIGURE 6. GAIN COMPRESSION

Typical Performance Curves (Continued)

Power Amplifier Temperature Performance NOTE: All data measured at $T_A = 25^oC$ and V_{G1}, V_{G2} and V_{G3} adjusted for first stage quiescent current of 20mA, second stage current of 50mA and third stage current of 90mA, respectively.

TBD

FIGURE 7. LINEAR GAIN

TBD

FIGURE 8. POWER OUTPUT

TBD

FIGURE 9. GAIN COMPRESSION

Power Amplifier Spurious Response at Various Supply Voltages NOTE: All data measured at $T_A = 25^oC$ and V_{G1}, V_{G2} and V_{G3} adjusted for first stage quiescent current of 20mA, second stage current of 50mA and third stage current of 90mA, respectively.

TBD

FIGURE 10. THIRD ORDER INTERMODULATION RATIO

TBD

FIGURE 11. SECOND HARMONIC RATIO

Typical Performance Curves (Continued)

TBD

FIGURE 12. THIRD HARMONIC RATIO

Transmit/Receive Switch Performance NOTE: All data measured with V_{DD} TR = +5V, $T_A = 25^oC$.

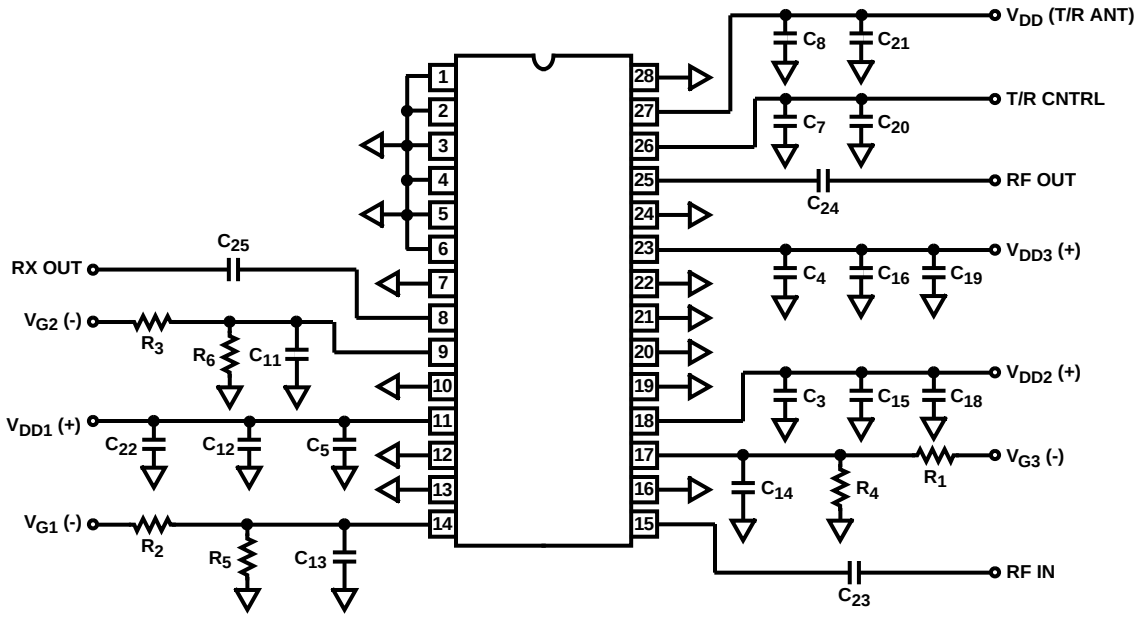
TBD

FIGURE 13. RECEIVE MODE T/R INSERTION LOSS/ISOLATION

TBD

FIGURE 14. RECEIVE MODE T/R SWITCH MATCH

Typical Application Example

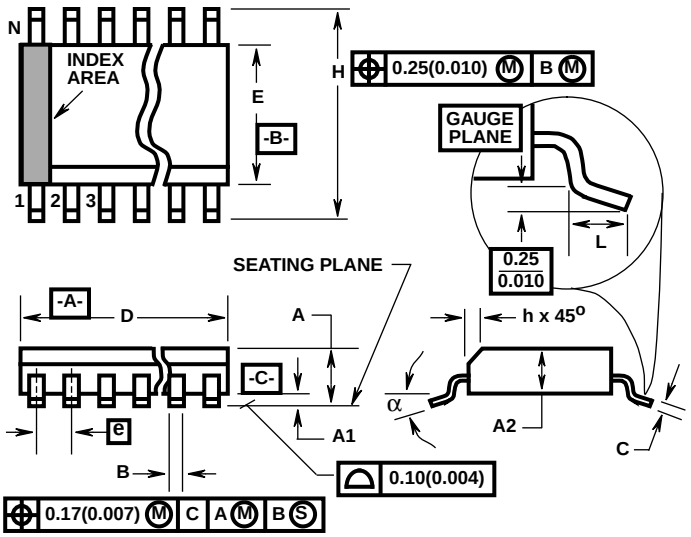


EXTERNAL CIRCUITRY PARTS LIST

LABEL	VALUE	PURPOSE
C_1 - C_6	22pF	Bypass (GHz)
C_{23} - C_{24}	22pF	DC Block
C_7 - C_{16}	1000pF	Bypass (MHz)
C_{17} - C_{22}	0.01µF	Bypass (kHz)
R_1, R_6	1.5kΩ	FET Gate Divider Network
R_3, R_5	5kΩ	
R_2	12kΩ	
R_4	1kΩ	

NOTE: All off-chip components are low cost surface mount components obtainable from multiple sources. (0.020in x 0.040in or 0.030in x 0.050in.)

Shrink Small Outline Plastic Packages (SSOP)



M28.15

28 LEAD SHRINK NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.053	0.069	1.35	1.75	-
A1	0.004	0.010	0.10	0.25	-
A2	-	0.061	-	1.54	-
B	0.008	0.012	0.20	0.30	9
C	0.007	0.010	0.18	0.25	-
D	0.386	0.394	9.81	10.00	3
E	0.150	0.157	3.81	3.98	4
e	0.025 BSC		0.635 BSC		-
H	0.228	0.244	5.80	6.19	-
h	0.0099	0.0196	0.26	0.49	5
L	0.016	0.050	0.41	1.27	6
N	28		28		7
α	0^o	8^o	0^o	8^o	-

Rev. 0 2/95

NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “B” does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm (0.004 inch) total in excess of “B” dimension at maximum material condition.
10. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.

All Harris Semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

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