

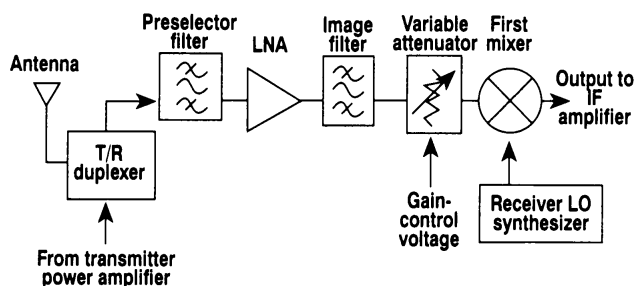
Integrated front-end components provide sensitivity and IMD control while operating under low-voltage/current conditions.

New digital communications systems integrate high-capacity wireless transceivers in packages as small as a PCMCIA card. Such transceivers rely on multifunction RF integrated circuits (ICs) to meet such rigid size requirements. Part 3 of this design series examines the role of RF ICs for high-performance wireless receiver front ends, particularly in hand-held systems.

Although the signal processing in many modern receivers occurs in the digital realm, analog circuits are still needed to amplify weak incoming signals from the antenna to a voltage which can be conveniently digitized. Direct conversion is the simplest receiver architecture. However, this approach places all filtering and detection processes at the signal frequency. Attractive from a cost and complexity standpoint, and adequate for less-demanding applications at lower frequencies, this technique does not provide adequate interference rejection in crowded bands. The method also fails to reject the noise close to the carrier characteristic of UHF and microwave oscillators used as receiver local oscillators (LOs).

Typically, communications receivers are constructed using a superheterodyne architecture (Fig. 1). The signal frequency is converted to a lower intermediate frequency (IF) in one or more steps for efficient amplification, filtering, and detection. Architectures using a single IF are often a good compromise when considering cost, size, and performance requirements.

The receiver is isolated from the transmitter and connected to the antenna through a duplexer. The duplexer may consist of band-splitting filters when the transmitter and receiver are sufficiently separated in frequency, such as in 900 MHz cellular telephone



1. This superheterodyne architecture is typical among wireless communication receivers.

systems. Alternately, the transmit/receive (T/R) duplexer may be a single-pole, double-throw (SPDT) switch when transmit and receive signals overlap or are too close in frequency to effectively filter, as may be the case in the 902-to-928-MHz band.

The typical superheterodyne receiver front-end circuitry consists of a band-limiting preselector filter (which may be part of the T/R duplexer), a low-noise amplifier (LNA), a mixer, and an LO. The gain ahead of the mixer may be controlled either by a variable-gain LNA or a voltage-controlled attenuator.

Successful receiver design optimizes the combination of sensitivity, interference rejection, overload protection, current consumption, size, and cost. In addition, battery-operated equipment must run at 3 V or less. Therefore, a number of design issues must be considered.

First of all, the LO and IF bands must be selected. Two frequency bands at the $LO \pm IF$ are converted to IF. The LO must be offset above or below the desired frequency by the IF. In addition to the desired frequency, an image frequency offset by twice the IF in the direction of the LO is also converted to the IF band.

A serious interference potential exists if the image response is not eliminated. Since the noise at the image frequency is also converted to the IF, the noise figure may be increased by 3 dB. The image signal may be filtered at any place ahead of the mixer. Placing the image filter just ahead of the mixer can lower the loss ahead of the LNA, reducing the overall system noise figure.

An alternate image-rejection technique is based on phase-cancellation techniques similar to single-sideband (SSB) generation. However, the rejection potential of the phase-cancellation method is difficult to realize because this technique relies on exact phase and amplitude tracking of two signal paths over temperature and time. For this reason, filters achieve much higher rejection in practice. Phase cancellation remains an interesting potential approach since it is more appropriate for monolithic implementation on an IC at low microwave frequencies than monolithic high-Q filters.

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The general IF choice is driven by IF and RF filter technology. The IF is chosen to be high enough so that the RF filters can reject the image frequency, but not so high as to unnecessarily increase the cost of the IF circuitry. The IF bandwidth and group delay must be matched to the characteristics of the received signal. Common communications receiver IFs are in the 10-to-100-MHz range. The exact IF is based on the frequency of potential interference sources and the LO synthesizer characteristics, among other considerations. Placement of the LO above or below the IF is based on the occupation of the resulting image bands and on LO synthesizer capabilities.

Receiver noise figure (NF) determines the receiver sensitivity in the absence of interference. The overall receiver NF will be the sum of duplexer loss, preselector loss, LNA NF, and mixer/IF amplifier noise according to:

$$F = F_{\text{dup}} + \left[\frac{(F_{\text{pre}} - 1)}{G_{\text{dup}}} \right] + \left[\frac{(F_{\text{ina}} - 1)}{G_{\text{dup}} G_{\text{pre}}} \right] + \left[\frac{(F_{\text{mix}} - 1)}{G_{\text{dup}} G_{\text{pre}} G_{\text{ina}}} \right] + \dots \quad (1)$$

While man-made noise and interference at 1 GHz may be equal to kTB or less in suburban or rural environments, noise in urban environments may be as much as 17 dB more than kTB and thus dominate the receiver system noise. In view of the other contributions to overall receiver noise level, LNA NF of 1.5 to 2.5 dB is adequate for most applications.

Potentially more important to receiver performance in the real-world operating environment is third-order intermodulation distortion (IMD). Odd-order IMD (of which third-order IMD is the largest) falls into the frequency band occupied by the desired signal and therefore cannot be eliminated by filtering techniques. Intermodulation products involving strong signals from nearby transmitters on adjacent and alternate channels can thereby mask a distant desired signal, even though the IF filter has adequate adjacent-channel rejection.

Intermodulation performance is usually specified in terms of the third-order intercept point (IP₃). This is the theoretical output power at which the extrapolated low-level third-order intermodulation products equal the two desired output signals. The value of IP₃ can be used to calculate the third-order intermodulation products given the level of two equal-amplitude signals according to:

$$IM_3 = 3P_{\text{signal}} - 2IP_3 \quad (2)$$

where:

P_{signal} = the power level of each test signal (in dB), and

IP₃ = the third-order intercept point (in dB).

IP₃ can be referenced to the input or the output by simply translating the value according to the linear gain.

The receiver mixer is particularly vulnerable to IMD due to the higher signal levels following the LNA. The problem is often alleviated by reducing the signal level to the mixer under strong signal conditions by means of a variable-gain LNA or variable attenuator between the LNA and mixer. Usually, two switched-gain or attenuation states are sufficient to obtain good intermodulation performance. The bulk of receiver signal-level control ahead of the detection process is relegated to the IF amplifier.

Better LNA and mixer intermodulation performance usually comes at the price of higher current drain -- the bane of battery-powered equipment. Thus, noise, intermodulation, and current drain cannot be simultaneously optimized. As a compromise, overall LNA/mixer gain is typically set at 20 to 25 dB, just high enough to remove IF amplifier noise from the overall receiver NF. Gain is typically distributed between the LNA and mixer according to the intermodulation and noise capabilities of the two blocks. The intermodulation performance is then maximized at the current drain, which can be tolerated by the system.

The impedance between component interfaces must be controlled to achieve optimum performance. The LNA NF, for example, is directly affected by the source impedance. Filter characteristics will also be affected by the terminating impedances at the input and output ports.

A clever choice of interface impedance can minimize receiver front-end current drain. High load impedance requires less current from a monolithic output buffer to produce a given voltage. Although filters at UHF and microwave frequencies are designed for use at 50 Ω, IF filters are available at terminating impedances as high as several thousand ohms.

The only method of matching high-impedance on-chip circuitry to a low impedance filter monolithically at IF is with an active buffer, which may consume more than half the total LNA/mixer current. Alternately, low-impedance

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filters can be matched to a high-impedance output port using external reactive components. Also, higher-impedance IF filters can be used.

Voltage as well as current-swing limits must be considered when setting the IF impedance level. The maximum peak-to-peak output voltage swing (V_{output}) is about $V_{\text{output}} - 1$ for resistive IF loads. Reactive matching networks can be used with open-drain output circuits to produce as much as $2V_{\text{output}} - 1$ peak-to-peak output swing. The optimum IF impedance (for minimum current drain) is a function of power-supply voltage and output IP_3 requirements. In other words, the same design considerations used to maximize efficiency in a power amplifier apply to low-signal-level circuits in the receiver as well.

As an example, assume no external-matching components are allowed, but a 50 Ω output drive capability is required from the output buffer. The output IP_3 (OIP_3) level is assumed to be 10 dB more than the maximum linear output power. The maximum linear output power is calculated from the maximum output current-voltage (I-V) swing by:

$$P_{\text{out(max)}} \equiv (V^+ - 1)^2 / 4R_L \quad (3)$$

and

$$OIP_3 \text{ (dBm)} \equiv 40 + 10 \log_{10} (R_L \times I_Q^2 / 2) \quad (4)$$

where:

R_L = the load impedance, and
 I_Q = the current consumption.

To produce a +12 dBm OIP_3 level, the output buffer must consume 8 mA. However, if the IF output load impedance can be raised to 500 Ω , the buffer current needs to be 2.5 mA for the same OIP_3 level. The voltage-swing limit in Eq. 3 restricts the 50 Ω output power levels to +13 and +19dBm, respectively, at power supplies of +3 and +5 VDC.

As another example, consider a case where reactive components can be used to transform the impedance. For a given power-supply voltage and desired current drain, there will be an optimum load resistance for the maximum output power and OIP_3 .

$$R_L \equiv (V^+ - 1) / I_Q \quad (5)$$

and

$$OIP_3 \text{ (dBm)} \equiv 40 + 10 \log_{10} [(V^+ - 1)(I_Q / 2)] \quad (6)$$

For example, 50 Ω transformed to 500 Ω at an open-drain IF output provides +16 dBm OIP_3 with only 4 mA current drain.

Finally, receiver current drain is minimized over time by simply placing the circuit in an idle mode when the receiver is not needed. Typical idle-mode current drain is between 10 and 100 μ A. The idle mode is activated by a CMOS logic line from the system controller.

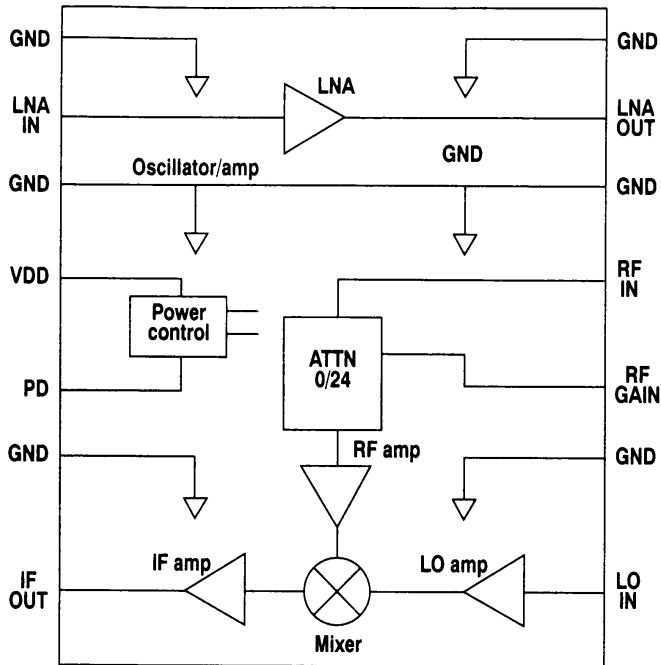
Receiver design can be simplified by combining front-end components, such as the LNA and mixer, into a single plastic SO-14 or SO-16 package. The LNA/mixer combination usually excludes the LO in order to meet the widest set of applications.

An example of such an LNA/mixer architecture (Fig. 2) contains all necessary receiver front-end functions except the LO and passive filtering. The IC (model RF2401) contains a high-dynamic-range LNA, a 1-bit digital attenuator to reduce mixer input level in the presence of strong signals, a second RF amplifier bundled with a double-balanced mixer, and an IF output buffer. The output of the LNA is available externally to permit optional insertion of a bandpass filter between the LNA and mixer.

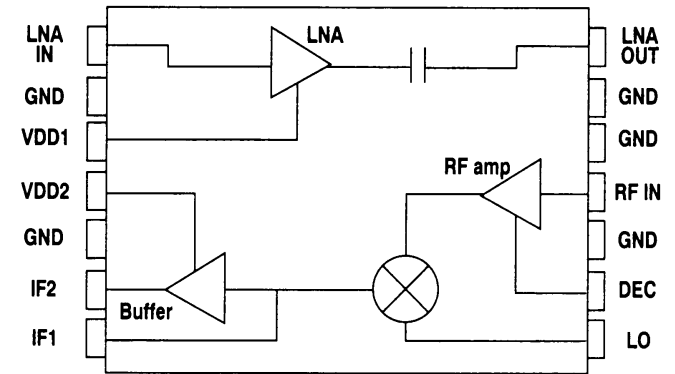
The LNA/mixer IC achieves 21 dB total gain and 3 dB noise figure in a 50 Ω system. It draws 30 mA from a +5 VDC supply with -7 dBm input IP_3 level. The IC incorporates a logic-controlled switch for 10 μ A idle-mode operation. No external-matching circuitry is required.

A similar circuit (Fig. 3) draws 15 mA from a power supply as low as +3 VDC with similar intermodulation and noise performance, as well as 18-dB gain in a 50 Ω system (model RF2418). The IC's output buffer can be connected in a high-impedance configuration to reduce current drain to only 6.5 mA. With a 500 Ω IF load, the total gain increases to 24 dB in this mode.

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2. This LNA/Mixer IC includes idle-mode power switching and a digital attenuator to reduce mixer-generated image signals.



3. This LNA/Mixer IC is optimized for minimum current drain at +3 VDC.

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