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Project Report

Low Phase Noise Voltage-Controlled Oscillator

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1 Introduction

Voltage-controlled oscillators (VCO's) are an integral part of phase-locked loops, clock recovery circuits, and frequency synthesizers. Random fluctuations in the output frequency of VCO's, expressed in terms of jitter and phase noise, have a direct impact on the timing accuracy where phase alignment is required and on the signal-to-noise ratio where frequency translation is performed. This project is concentrated on low phase noise VCO design.

2 A Study of Phase Noise in CMOS Oscillators

Phase noise is important in wireless communications. It can corrupt the signals in the nearby channels. There are three types of VCO that are commonly used: LC tank, relaxation and ring oscillators. The ring oscillators are the most suitable for integration. As a result, it is the most promising candidate for monolithic VCO's.

The noise can be itemized as follows:

- additive noise
- high-frequency multiplicative noise
- low-frequency multiplicative noise
- cyclostationary noise sources
- power supply and substrate noise

3 Comparison between Three Types of Loads

There are three different types of loads that are commonly used in VCO's, which are shown in Fig. 1. (a) is diode connected transistors, (b) is resistors and (c) is transistors in triode.

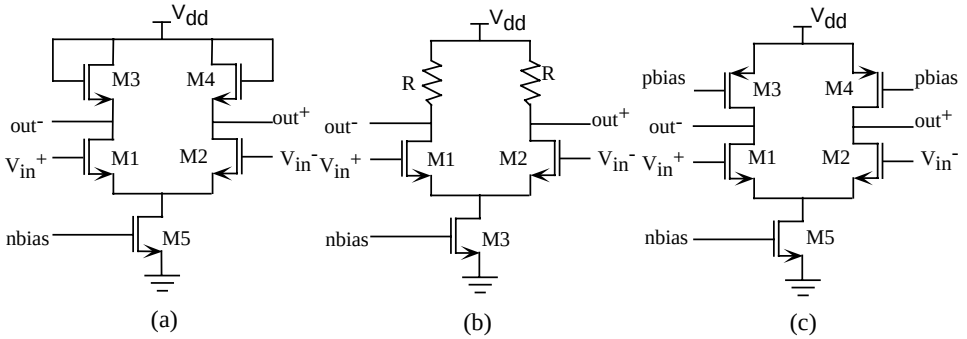

Figure 1: Three different types of loads (a) diode connected MOS (b) resistor (c) MOS in triode

If the diode connected transistors are used as load, the gain of each stage can be written as

$$A_0 = \frac{g_{m_{M1}}}{g_{m_{M3}}} = \sqrt{\frac{(W/L)_{M1}}{(W/L)_{M3}}} \tag{1}$$

which is only a function of the transistor geometry. This greatly simplifies the design. In case of resistors as a load, the gain is given by

$$A_0 = g_m R = \sqrt{\frac{k_n I_{SS} W}{L}} R \tag{2}$$

where I_{SS} is the tail current. If the load is transistors in triode, the gain can be expressed by

$$A_0 = \frac{g_{m_{M1}}}{g_{ds_{M3}}} = \frac{\sqrt{k_n I_{SS} W/L}}{k_p \frac{W}{L}(V_{gs} - V_T - V_{ds})} \tag{3}$$

Fig. 2, Fig. 3 and Fig. 4 show the frequency, peak-to-peak voltage and the largest derivative of the output waveform as a function of the tail current with three different types of loads. It is interesting to note that for the diode connected load, as the current grows larger, all its characteristics tend to saturate. This implies that if the VCO is operated in this region, it is insensitive to its bias and, as a result, reject the DC and low frequency noise from the bias.

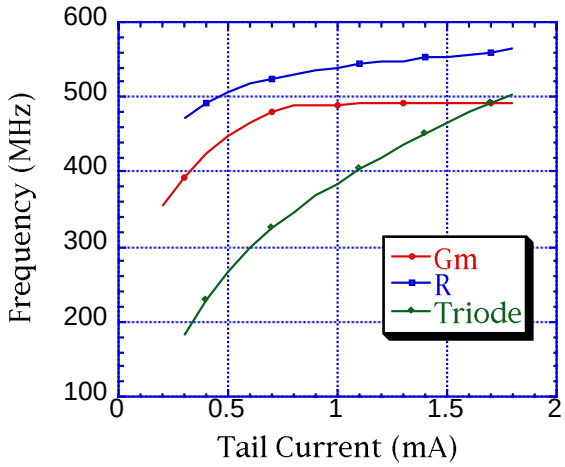

Figure 2: Running frequency as a function of the tail current

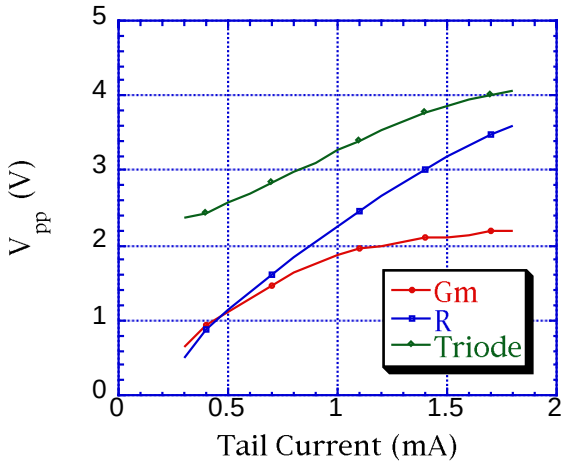

Figure 3: Peak-to-peak voltage as a function of the tail current

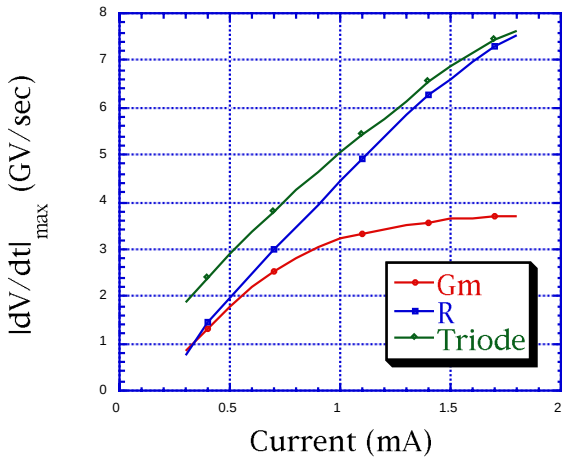

Figure 4: The largest derivative of the output waveform as a function of the tail current

4 Minimum Gain

To make the VCO oscillate at certain frequency, the gain of delay cells at that frequency must be greater than 1. However, there is always a trade-off between gain and bandwidth of an amplifier. An exceedingly large gain would limit the maximum operating frequency of the VCO. Moreover, the timing jitter becomes larger when the gain of the delay cell is large. For this reason, an amplitude limiting NMOS transistor is inserted between the output nodes, which is shown is Fig. 5[1]. The common source of input transistors is assumed to be virtual ground. In reality, this node oscillates at the output frequency with the amplitude depending on the input voltage V_{in}.

If the signal is fed through the capacitor C_{gd} to the gate of current bias transistor, the bias current may be affected and cause drift in the output frequency. The feedthrough problem can be reduced if the output oscillation amplitude can be limited. This can be achieved by inserting a transistor $M5$ between the output nodes with the gate connected to the positive supply voltage.

In addition to reducing the feedthrough, the use of the limiting transistor also helps smooth out the VCO output waveform and save a significant amount of power. This is due to the nonlinear and signal dependent load transistor. Without a swing limiter, for a large input, one of the outputs

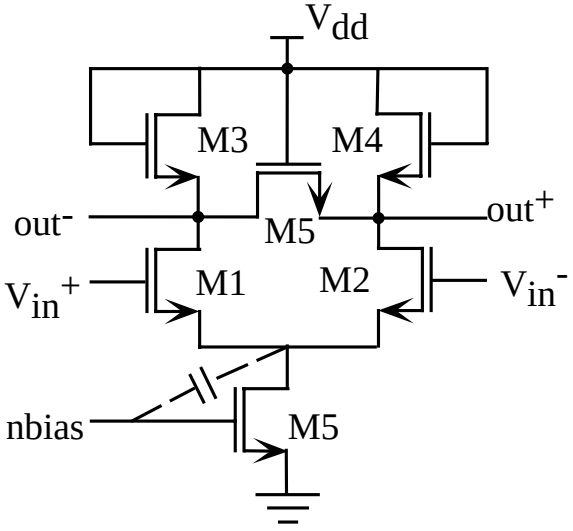

Figure 5: An inverter stage with gain limiting transistor

of the delay cell may keep increasing. With a limiter, a lower swing can be obtained and hence increase the oscillating frequency. So a certain frequency can be reached with less tail current by inserting the swing limiter.

Fig. 6, Fig. 7 and Fig. 8 show the comparison between the inverter stages with and without the swing limiter in terms of the oscillating frequency, peak-to-peak voltage and the largest derivative of the waveform as a function of the tail current.

5 Mathematical Modeling

In general, VCO is a highly nonlinear system where linear analysis cannot apply. However, if the amplitude is small enough, small signal model is still valid and the analysis is greatly simplified. As the amplitude grows larger, the system becomes nonlinear. The resulted error has to be check be testing.

If each stage of the VCO is modeled as a single-pole system with the small signal model shown in Fig. 9. The transfer function is given by

$$H(s) = \frac{V_{out}}{V_{in}} = -\frac{g_m R}{1 + sRC} \tag{4}$$

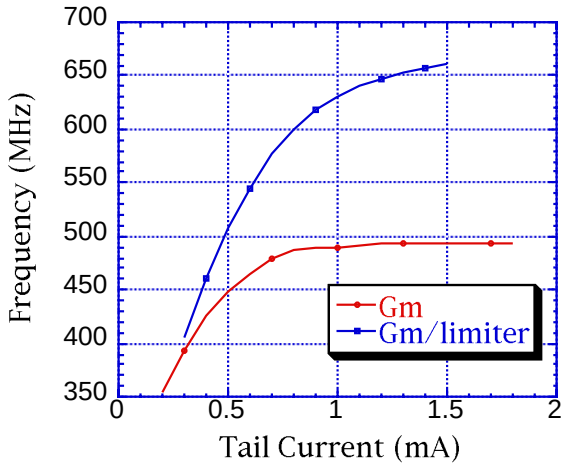

Figure 6: Oscillating frequency as a function of the tail current with and without the swing limiter

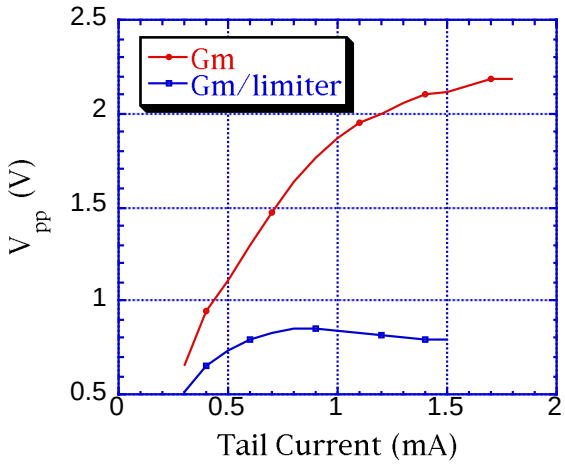

Figure 7: Peak-to-peak voltage as a function of the tail current with and without the swing limiter

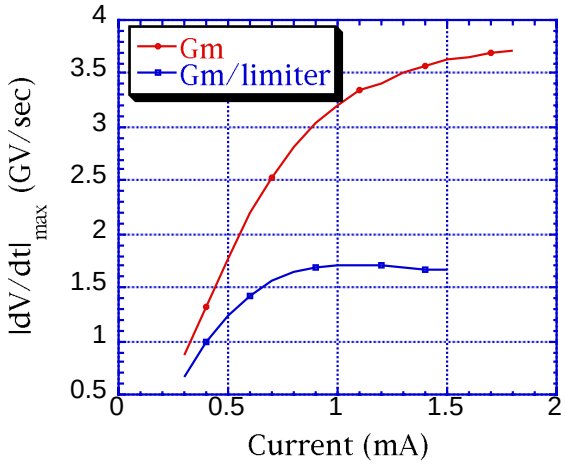

Figure 8: The largest derivative of the output waveform as a function of the tail current with and without swing limiter

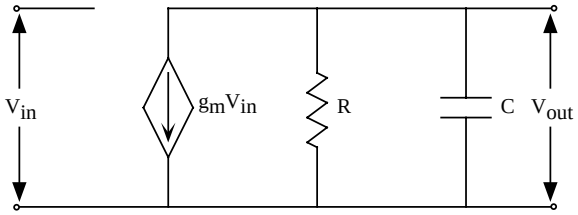

Figure 9: Single stage small signal model

Considering even number of stages, which has the advantage of supplying I and Q simultaneously, the delay of each stage is given by

$$\phi = \frac{\pi}{N} = \arctan(2\pi f RC) \tag{5}$$

where f is the oscillating frequency. So f can be expressed in terms of R, C and N as

$$f = \frac{\tan(\pi/N)}{2\pi RC} \tag{6}$$

Note that R can be either $1/g_m$, resistance or $1/g_{ds}$, depending on the type of the load, which implies that the running frequency can possibly be a function of the current.

At this point, if we assume that g_m is large enough so that the current waveform looks like a square wave. The load capacitor at each stage is

charged from $-V_{pp}/2$ up to $V_{pp}/2$ during half of a period. So the peak-to-peak voltage swing can be given by

$$V_{pp} = I_{SS}R(1 - e^{-\frac{1}{2fRC}}) = I_{SS}R(1 - e^{-\frac{\pi}{\tan(\pi/N)}}) \tag{7}$$

Since the largest phase error occurs at the zero crossings where the waveform has the largest derivative, we need to look at the largest derivative $|\frac{dV}{dt}|_{max}$. Assuming the waveform is sinusoidal, the largest derivative is given by

$$|\frac{dV}{dt}|_{max} = \omega V_{pp} = 2\pi f I_{SS}R(1 - e^{-\frac{\pi}{\tan(\pi/N)}}) \tag{8}$$

The noise contribution in terms of the maximum jitter time τ is given by

$$\tau = \frac{V_n}{|dV/dt|_{max}} \tag{9}$$

From Eqn(8) and Eqn(9), we can see that as N increases, the jitter noise decreases. However, when N gets too large, the term $e^{-\frac{\pi}{\tan(\pi/N)}} \approx e^{-N}$ becomes negligible. In other words, after a certain point, increasing the number of stages can hardly reduce the jitter noise. On the other hand, each stage contributes extra noise to the output spectrum. Besides, the tail current has to be increased substantially in order to compensate for the extra delay of each stage. As an example, if the current remains a constant, when the number of stages increases from 3 to 4, τ is reduced by a factor of 0.23. However, when the number of stages is increased from 4 to 6, τ is only reduced by a factor of 0.08. So the optimal number of stages is around four.

From another point of view, the Q factor of the oscillator is defined by [2]

$$Q = \frac{\omega_0}{2}\sqrt{(\frac{dA}{d\omega})^2_{\omega_0} + (\frac{d\Phi}{d\omega})^2_{\omega_0}} \tag{10}$$

where A and Φ are the magnitude and phase response of the open loop transfer function of the oscillator respectively, and ω_0 is the oscillating frequency in rad/sec. The noise power spectral density is shaped by $\frac{1}{4Q^2}(\frac{\omega_0}{\Delta\omega})^2$. By adding more stages, we are essentially increasing $\frac{dA}{d\omega}$ and $\frac{d\Phi}{d\omega}$ and hence increasing the Q factor. So the noise contribution becomes less. However, while we add more stages, we are also adding more noise associated with each stage. So there is a clear trade-off between the two.

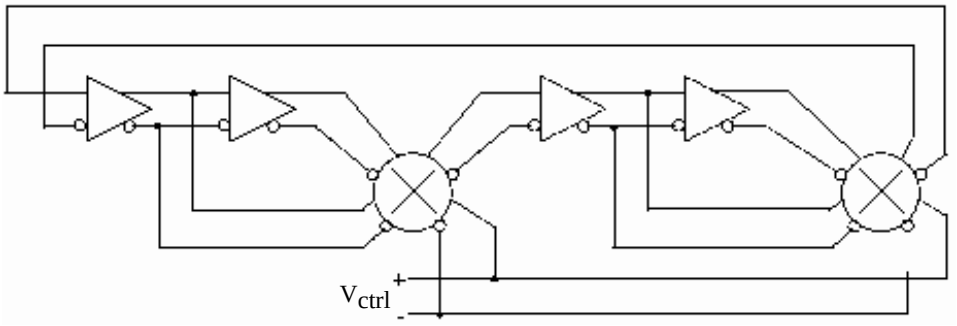

Figure 10: Block diagram of a interpolating VCO

6 VCO Design

The VCO operating at 622MHz is implemented with interpolating ring structure as shown in Fig. 10[3]. Each stage is an fully differential inverter as shown in Fig. 5. An interpolating ring VCO is one whose delay-per-stage is fixed and the output frequency is controlled by interpolation between adjacent delay cells[4]. A Gilbert multiplier acts as the interpolating circuit which is shown is Fig. 11. Fig. 10 also illustrates the output of the interpolater as the weighted sum of its inputs. By changing the weighting distribution with a control voltage, a continuously variable delay is produced.

$$V_{out} = xV_{late} + (1-x)V_{early} \tag{11}$$

Notice that the equivalent delay of only two of the four unit delays is adjusted by interpolation. Therefore, the maximum possible tuning range is from 2 to 4 delays of each inverter plus the delays of the interpolaters. Since the frequency can be tuned without changing the operating point of each stage, a more linear and wider tuning range can be achieved.

A temperature compensated biasing circuitry is implemented with the diagram shown in Fig. 12, the opamp in which is realized with a simple structure as shown in Fig. 13[3]. An output current, I_{out}, which flows through R, is given by

$$I_{out} = \frac{1}{R^2}\frac{1}{\frac{1}{2}\mu_p C_{ox}}(\sqrt{\frac{L_2}{W_2}} - \sqrt{\frac{L_1}{W_1}})^2 \tag{12}$$

The resulting current is inversely proportional to the mobility μ_p. Rewrite

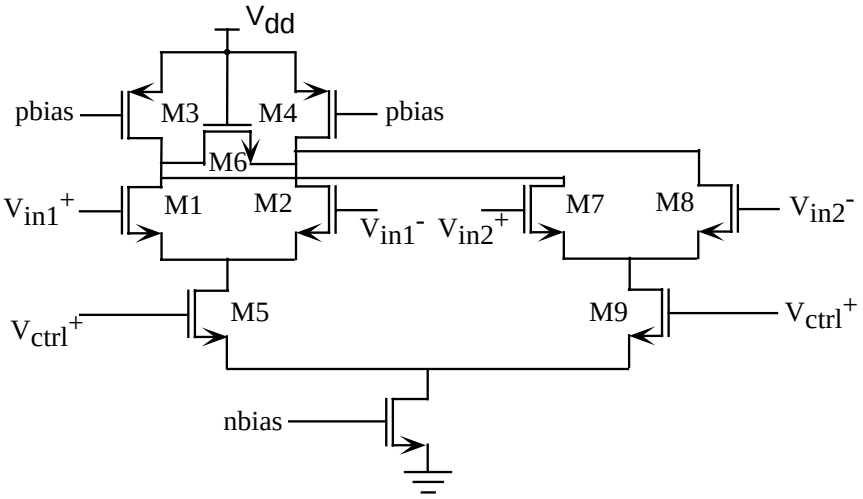

Figure 11: Schematic of the delay cell

Eqn. 6

$$f = \frac{\tan(\pi/N)}{2\pi RC}.$$

In our case, the load is diode connected transistors. We have

$$R = \frac{1}{g_m} = \sqrt{\frac{L}{I_{SS}\mu_p C_{ox} W}} \tag{13}$$

So

$$f = \frac{\sqrt{\frac{I_{SS}\mu_p C_{ox} W}{L}}\tan(\pi/N)}{2\pi C} \tag{14}$$

Now that we maintain $I_{SS}\mu_p$ as a constant, the frequency drift due to the temperature variation is greatly reduced.

7 Simulation Results

Fig. 14 illustrates the voltage-to-frequency relationship of the VCO at room temperature by simulation. A linear tuning range between 574MHz and 891MHz is achieved with a VCO gain of 213MHz/V. Fig. 15 illustrates the peak-to-peak voltage as a function of the control voltage. It varies from

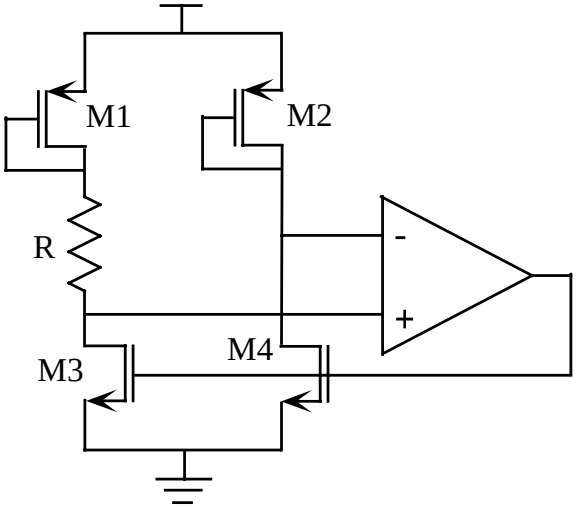

Figure 12: Circuit of temperature compensated biasing

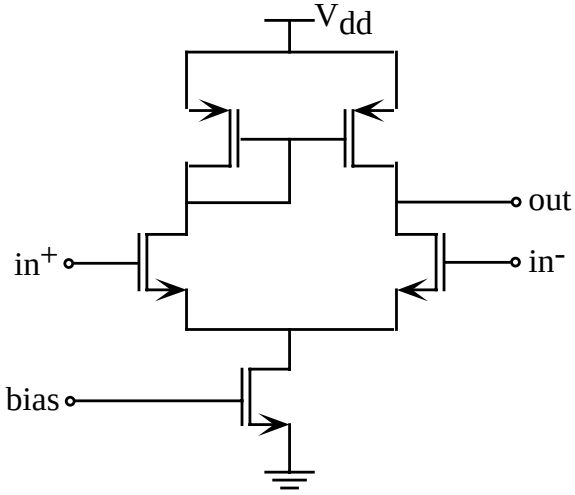

Figure 13: Diagram of the opamp

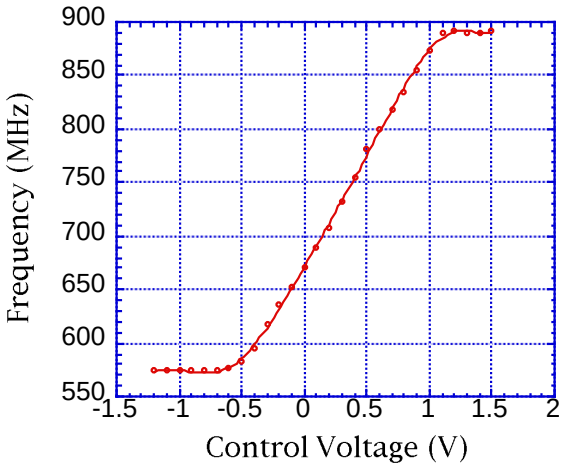

Figure 14: Output frequency against control voltage

0.618V to 0.164V as the frequency is tuned. Fig. 16 shows the free-running frequency variation due to the temperature drift. From the curve fitting, we can see that the temperature coefficient is $-0.92MHz/^oC$. This is not as good as the result given in the reference paper, but it is good enough for not interfering with the frequency tuning.

8 Conclusion

The different noise in VCO has been studied. Three types of loads are compared. The optimal number of stages in a ring oscillator is determined to be around 4 with mathematical modeling. A 622MHz interpolating ring VCO has been designed with temperature compensated biasing. The chip will be fabricated with $0.5\mu m$ technology and be tested later.

References

[1] Shing-Tak Yan and Howard C. Luong. "A 3 V 1.3-to-1.8 GHz CMOS Voltage-Controlled Oscillator with 0.3 ps-Jitter". In *Proc. ISSCC*, page ?, 1997.

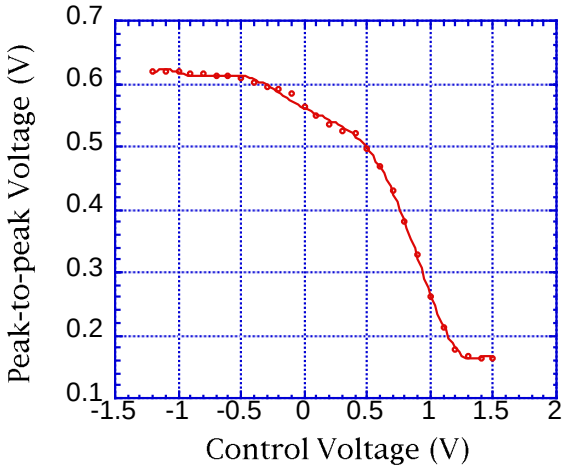

Figure 15: Output peak-to-peak voltage against control voltage

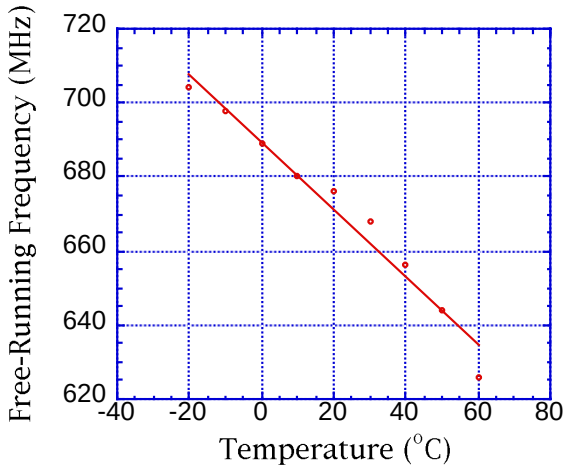

Figure 16: Center frequency against temperature using temperature compensated biasing

[2] Behzad Razavi. "a Study of Phase Noise in CMOS Oscillators". *IEEE J. Solid-State Circuits*, Vol. 31(No. 3):pp.331–343, March 1996.

[3] Wing-Hong Chan, Jack Lau, and Aaron Buchwald. "A 622-MHz Interpolating Ring VCO with Temperature compensation and Jitter Analysis". In *Proc. ISSCC*, page ?, 1997.

[4] J. A. McNeill. "Interpolating Ring VCO with V-to-f Linearity Compensation". *Electronics Letters*, Vol. 30(No. 34):pp.2003–2004, Nov. 1994.