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News Briefs

MAXIM REPORTS RECORD REVENUES, EARNINGS, AND OPERATING INCOME FOR THE SECOND QUARTER

Maxim Integrated Products, Inc., reported record net revenues of $106.2 million for the second quarter of fiscal 1996 ending December 31, 1995, compared to $56.2 million for the same period a year ago. This represents an 89% increase in net revenues from the same quarter a year ago. This growth rate is the result of the Company's manufacturing efforts to get shipping levels more in line with customer booking and usage rates. Net income increased 258% to $31.9 million (or $0.45 per share) for the quarter, compared to net income of $8.9 million (or $0.14 per share) for the same quarter in fiscal 1995. Bookings across all product lines continue to exceed shipments. Backlog shippable in the next 12 months remains at over $190 million. Operating income was a record 45.1% of net revenues, compared to 23.5% for Q295. Annualized return on equity increased to 58.4% for Q296 compared to 25.2% for fiscal 1995.

These results mark our 41st consecutive quarter of increased revenues and 39th consecutive quarter of increased earnings, a record unmatched by any company in the analog integrated circuit industry.

During the quarter, the Company increased cash and short-term investments by $6.2 million after paying for over $21 million in capital equipment and repurchasing $15.6 million of its common stock.

Factory shipments for the first 6 months of fiscal 1996 increased 88% as compared to the same period in fiscal 1995. Wafer fabrication production increased 124% over the same period in fiscal 1995. However, revenues reported for the quarter continue to be constrained by wafer fabrication production levels.

Jack Gifford, Chairman, President, and CEO, commented: "While Maxim built and shipped 88% more product during the first 6 months of fiscal 1996 than during the same period in 1995, it has been more difficult than planned to increase production levels at our Beaverton wafer fabrication facility. Productivity levels, as measured by quarterly wafers out per technician, reached a peak in Q495 and were essentially flat in the first half of FY96. The Beaverton facility's production efficiency is currently 50% of Maxim's Sunnyvale facility."

Mr. Gifford commented further: "During the first two quarters after we acquired the facility from Tektronix, we were able to take advantage of 60 trained technicians acquired with the facility. Since that time, we have added over 150 technicians who were untrained in our wafer manufacturing processes and equipment. Although we believe that these technicians have accomplished a great deal in a short time, we anticipate that it will be several quarters before they will be fully trained and approaching the efficiency levels of our Sunnyvale facility. The availability of trained technicians in the Portland area has not been sufficient to meet our plan for manufacturing capacity."

Gifford continued: "Based on this experience in Beaverton, I believe that the lack of qualified, trained technicians worldwide could be a challenge to the industry as the planned wafer capacity comes on line in 1996 and beyond. This factor, along with continued increased worldwide demand, will continue to put pressure on those facilities that are up and running today."

During the quarter, the Board of Governors of NASDAQ added Maxim to its index of NASDAQ 100 companies. This positions Maxim as one of the top 100 issues traded on the NASDAQ today.

Comparator/DAC combinations solve data-acquisition problems

The following discussion examines an overlooked option for many existing A/D converter applications: the A/D conversion is sometimes better implemented with a discrete comparator and D/A converter. This substitution generally entails a different measurement approach, but the advantages can include lower cost, higher speed, more flexibility, and lower power consumption.

Current trends, though, are in the other direction—designers who must implement A/D conversion usually specify a packaged A/D converter (ADC) for the job. Most engineers are not aware of an alternative, and the price/performance ratios for ADCs are falling all the time. Yet, an analog comparator plus D/A converter (DAC), along with digital processing capability, form the core of a successive-approximation ADC.

The discrete comparator/DAC approach is already common in certain fields. Automatic test equipment, nuclear pulse-height discriminators, and automated time-domain reflectometers often use the technique whereby one comparator input is driven by the DAC, and the other is driven by the signal to be monitored. Following is a selection of general measurement problems and specific applications in which a comparator/DAC combination is actually more appropriate than an off-the-shelf ADC.

Transient voltage analysis

A brute-force technique for capturing fast-changing amplitude events (transients) is simply to digitize them with a high-speed ADC supported by a processor and fast RAM (**Figure 1**). Single-shot events may compel the use of this approach, as may the need to discern fine detail in the transients. Otherwise, if the transients are repetitive, you can measure their peak amplitude and other features with the DAC/comparator approach (**Figure 2**).

The DAC sets a trial level at one input of the comparator while the transient signal is applied to the other input. You then determine peak transient amplitudes by adjusting the DAC output, using a digital latch to capture the comparator's output response when its threshold is exceeded. Only the comparator input need sustain the full

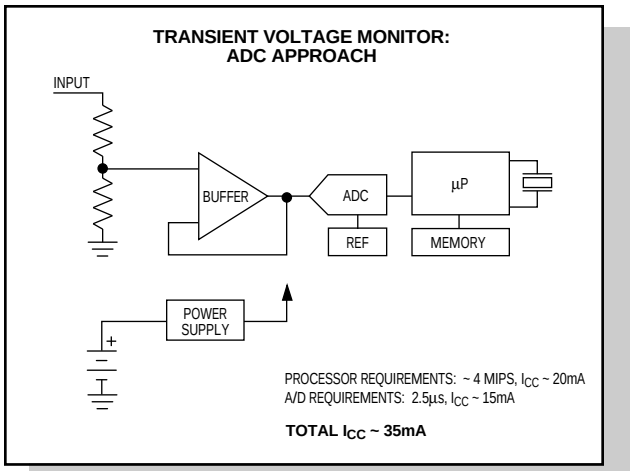


Figure 1. As the brute-force approach to transient analysis, an ADC circuit is power-hungry and expensive.

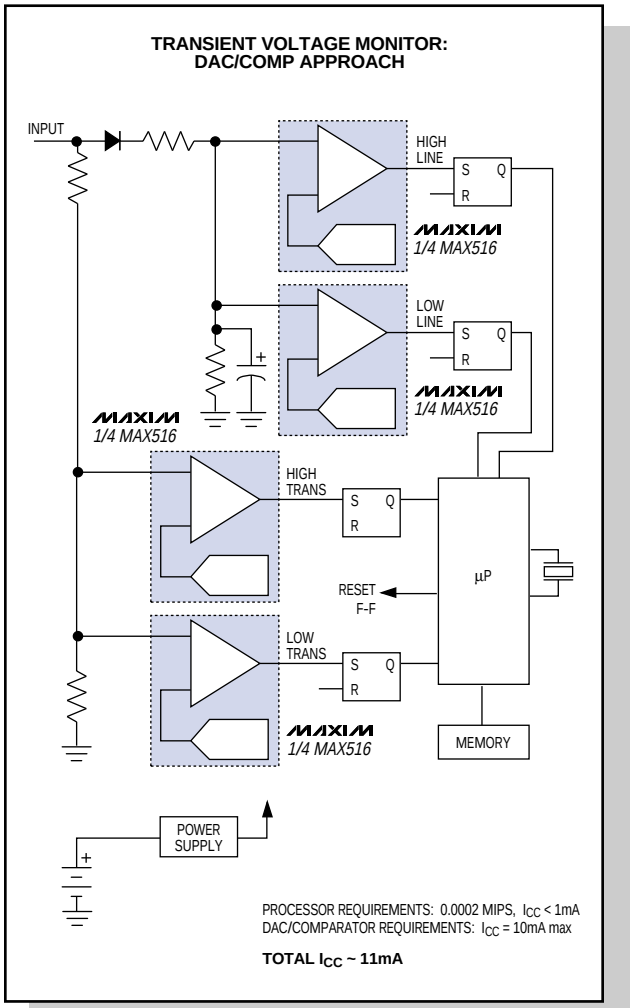


Figure 2. If the Figure 1 application can accept an iterative approach to the amplitude measurements, replacing the ADC with DAC/comparator combinations saves power and cost.

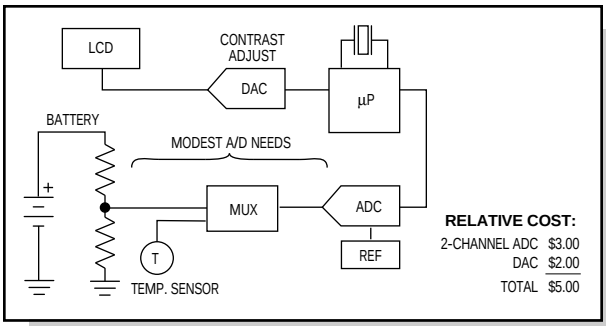


Figure 3. This circuitry is commonly found in portable instruments.

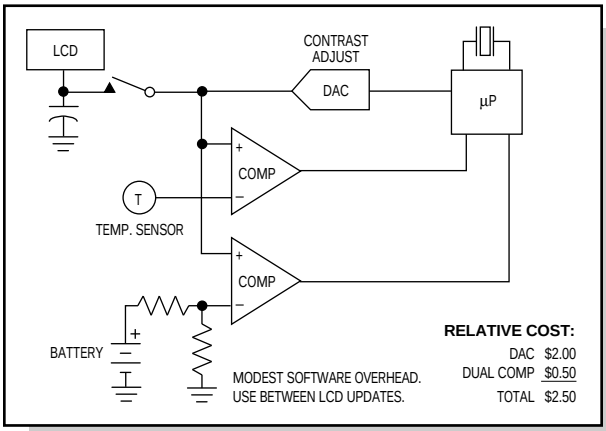


Figure 4. Adding two comparators to the circuit of Figure 3 enables the DAC to double as an ADC, saving cost.

bandwidth of the transient, and the DAC output can exhibit arbitrarily long settling times without affecting the measurement accuracy. Thus, sensing in the analog domain lets you replace an expensive ADC with a low-cost DAC and comparator.

A related problem is monitoring an analog voltage with respect to tolerance limits. Many self-diagnostic instruments monitor system voltages, temperatures, and other analog quantities against limit values set in software. However, if the comparisons are made by a comparator whose setpoint value is provided by a DAC, you can reduce the processor's overhead because it need only read a single bit representing the out-of-limit condition.

This technique (analog-domain comparison) is just as accurate as the ADC technique (digital-domain comparison), so why digitize the whole value when you can simply compare it against a setpoint? One case should be mentioned: If the value must be compared against several setpoints, such as a low and high warning level and a low and high shutdown level, an ADC may be preferable to the four DACs and four comparators otherwise required.

Derive a simple ADC from an existing DAC

In portable instruments constrained by cost and size, an existing DAC can sometimes be persuaded to perform A/D conversions as well. Cellular phones and medical electronics, for example, often include a DAC for adjusting the contrast voltage in an LCD (**Figure 3**). In some cases you can also monitor a temperature or battery voltage (as described above) simply by adding a comparator and switches. The existing DAC then does double duty, with the display blanked while the DAC participates in analog-to-digital conversions. As an alternative to blanking, a simple sample/hold consisting of an analog switch and capacitor (**Figure 4**) can maintain the LCD contrast voltage during an A/D conversion.

Another alternative is to substitute a low-cost dual DAC for the existing single DAC. One half of the dual DAC produces a full-time LCD-contrast voltage, while the other half helps form a full-time ADC. Whether single or dual, the DAC and comparator require support from a fast, simple software routine that drives the DAC and samples the comparator to implement successive approximation (see **sidebar**, *Successive Approximation*).

Design considerations

Combining a DAC and comparator is simple. A signal is applied to the comparator's noninverting input, and the DAC provides a digitally programmable threshold at the inverting input. The comparator then produces a logic-high output whenever the signal is more positive than its threshold. But, you must apply care in several areas.

To ensure accurate threshold levels, the DAC's dc output resistance should be low with respect the the comparator's input bias current and scaling network. This concern arises mainly in very low-power circuits, for which the DAC's output resistance can be as high as 10kΩ.

Another DAC requirement is low ac output impedance. Otherwise, the comparator output's fast digital slew rate can couple through parasitic layout capacitance, producing input transients that degrade accuracy by causing oscillation. If some settling time can be sacrificed, you can lower the DAC's ac output impedance by adding a bypass capacitor at the comparator input. Instability and oscillation can result from too much capacitive load on the DAC's output amplifier, but that problem is easily fixed by adding a resistor in series with the DAC output.

The main issue for comparators is hysteresis. Most comparator circuits include hysteresis to prevent noise and oscillation, but hysteresis should be used sparingly—

DAC/Comparator Combo ICs

Maxim offers three monolithic devices that greatly simplify a design by combining the functions of a comparator and a DAC. Each device is suitable for the applications in this article, as well as many others.

The MAX516, for example, is a quad device with sub-microsecond speed, suitable for many medium-speed, multiple-channel applications (**Figure S1a**).

The MAX910 is a single, high-speed, TTL-output DAC/comparator with 8ns propagation delay (**Figure S1b**). A similar device (the MAX911) is even faster—it has complementary-ECL outputs and a propagation delay of 4ns.

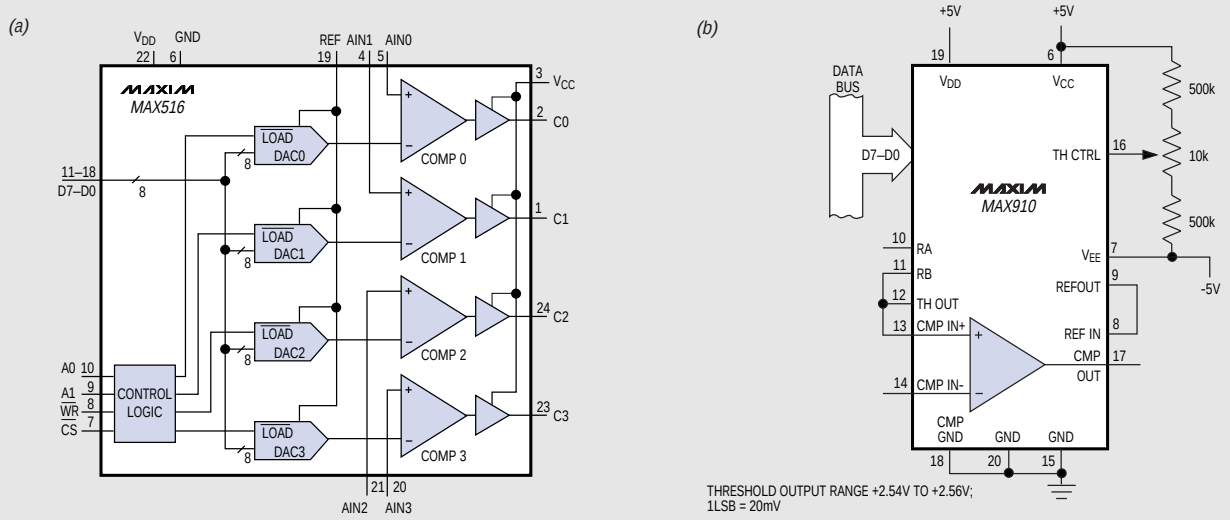


Figure S1. 8-bit DAC/comparator ICs from Maxim include the quad MAX516 (a), the high-speed, TTL-compatible MAX910 (b), and the ECL-compatible MAX911 (not shown).

Successive Approximation

Successive approximation is easily illustrated by the procedure that uses a balance and a set of binary trial weights (a series of weights whose relative values are 1, 2, 4, 8, 16, etc.) to determine an object's weight. To determine the unknown weight by the quickest method (successive approximation), first balance the unknown against the largest trial weight. According to the balance indication, either remove that weight or add the next largest, and continue that process down to the smallest trial weight. The resulting best estimate of the object's weight is the sum of trial weights remaining in the balance pan.

In successive-approximation ADCs, the bits of the internal DAC are analogous to the set of binary weights, and the comparator output is analogous to the balance indication. Logic for driving the bit-trial procedure can reside either in the successive-approximation register (SAR) of a packaged ADC, or in a software routine associated with the processor that controls a DAC/comparator circuit. The "pseudo-code" shown in Table S1 represents such a routine. For most processors, this routine can be realized with fewer than 20 lines of code.

Table S1. Pseudo-Code for Successive Approximation

Begin:	/Comments
Mask = 80h	/Shifting weight value—start high
Value = 80h	/Value = output (initially half scale)
Loop:	
Output DAC (Value)	/Output current Value to DAC
Delay (settling time)	/Wait for DAC output to settle
If input (comp. output) = high	/Check comparator output bit
Value = Value and not (mask)	/Clear mask bit (set by default)
Shift mask right:	
Value = Value or mask	/Next trial weight
Loop until mask = 0	/Loop until all bit weights are tried
End: Value contains the final result of the successive approximation.	

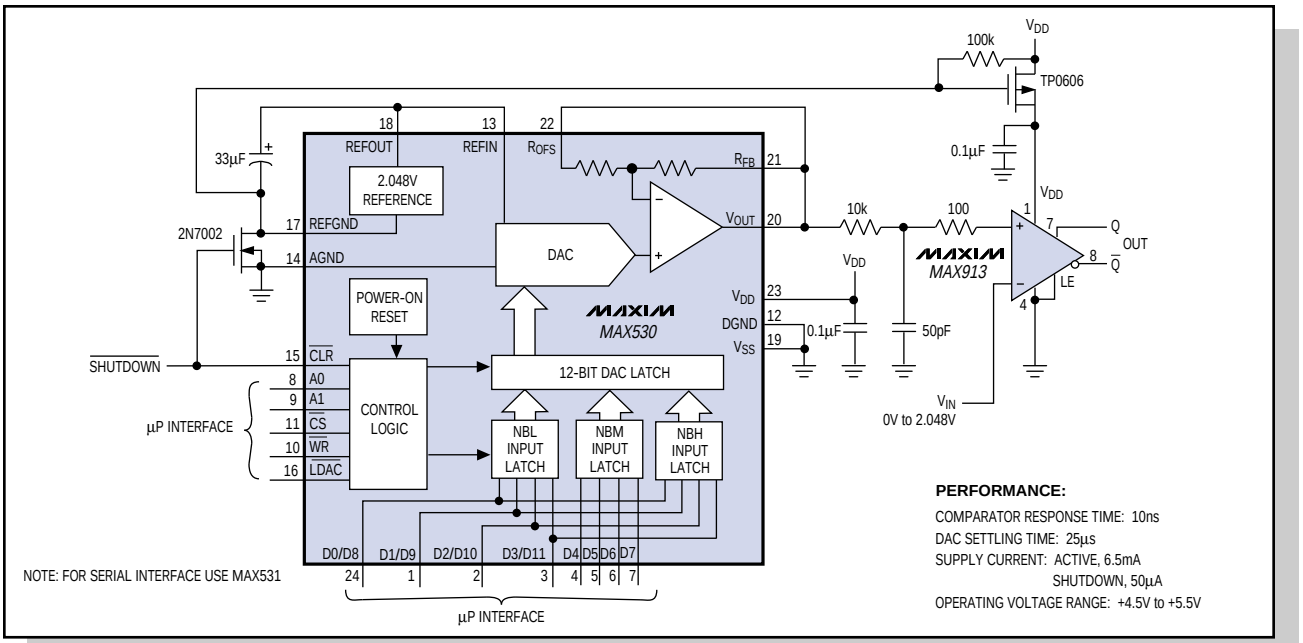


Figure 5. Because the comparator is stable in its linear region, this high-speed, 12-bit amplitude digitizer can handle slow-moving input voltages without oscillation.

it also causes the threshold value to change with output state. That behavior is acceptable if the system can compensate for state-dependent hysteresis; otherwise hysteresis should be avoided.

If the comparator to be used has internal hysteresis that cannot be disabled, you can eliminate any negative effect by ensuring that the DAC output always approaches the comparator threshold from the same direction. That action is easily established by setting the DAC to zero after each bit test; i.e., by adding one line to the pseudo-code listing at the end of this article (see sidebar, *Successive Approximation*).

As another option, you can often eliminate the need for hysteresis by adding a small amount of capacitive feedback, which provides speedup in the comparator's linear-transition region. Or, you can add an output flip-flop or latch to capture the comparator's output state at a given instant of time.

Modern comparators are better able to handle input signals that have a limited slew rate. The MAX913 and MAX912 from Maxim, for example, are particularly effective in this respect because they are actually stable in their linear regions. **Figure 5** illustrates the MAX913's performance in a high-speed, 12-bit application. As another DAC/comparator example, the **Figure 6** circuit (an ultra-low-power 8-bit converter) conserves power by turning itself off when not in use.

Applications

This section presents a number of situations in which a DAC/comparator approach offers advantages over the ADC approach. The application circuits discussed are neither unusual nor esoteric, but address common problems that arise frequently.

First, consider the need for a low-cost method to detect and log the sags, surges, and transients that occur on a power line. An ideal design would be a wall-cube device that detects power-line abnormalities and logs the time of each occurrence to RAM. (Sags and surges can last from milliseconds to hours; transients are as short as 10 microseconds.) The monitor must log the duration of complete failures in line power, so the monitor power should come from a battery.

The conventional solution to this problem is a controller and ADC converter. As the converter continually samples the line voltage, the controller compares each value to user-settable limits stored in software, and logs any out-of-spec condition to RAM. Because the system must be capable of tracking transients as brief as 10µs, the ADC sample interval must be considerably shorter—perhaps 2.5µs maximum as a conservative estimate. The controller must therefore process the samples at 1/2.5µs = 400ksps.

If software comparisons can be coded efficiently and the ADC requires no processor intervention, this system can operate with as few as ten instructions per sample,

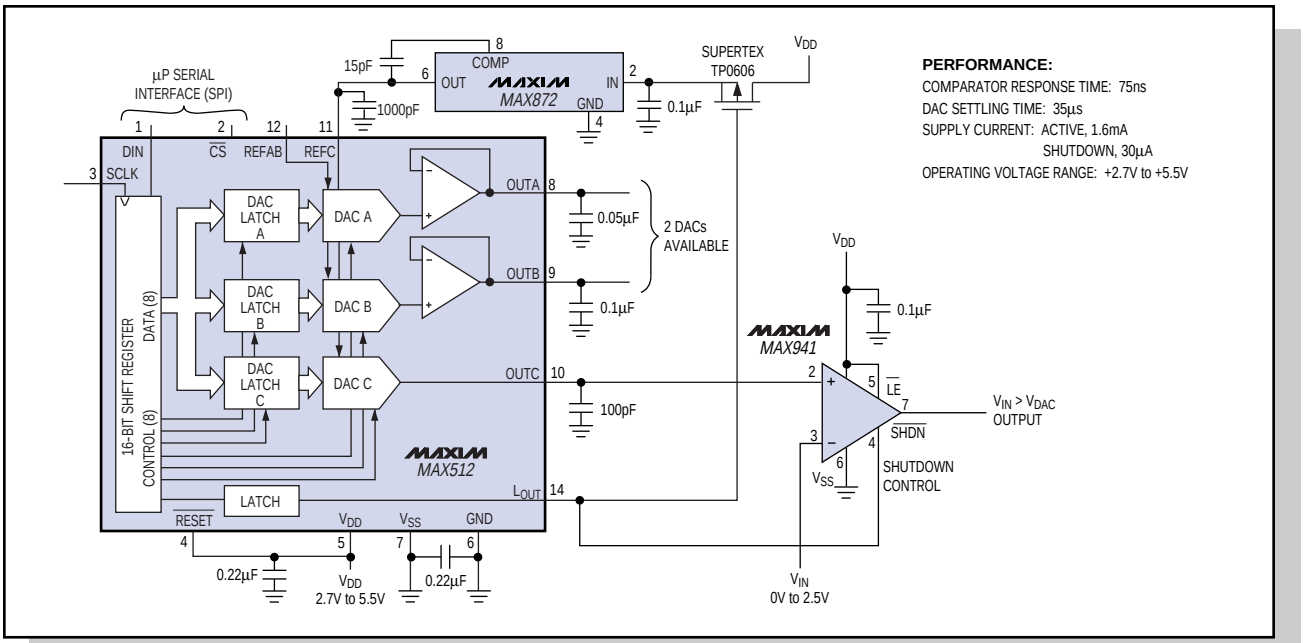


Figure 6. This low-voltage, 8-bit digitizer offers several advantages over the ADC alternative: low cost, low power consumption, and between-sample shutdown capability.

requiring processor performance in the 4 MIPS range. Such performance is substantial, and is not readily compatible with battery operation (Figure 1). You might then consider an analog method that responds to the derivative of an input transient instead of tracking it, but that approach appears untenable.

The alternate DAC/comparator approach in this case offers several significant advantages. It requires four DACs and four comparators (or a single MAX516), followed by a quad set/reset flip-flop. One DAC/comparator/FF combination monitors high transients, one monitors low transients, one is for sags, and one is for surges (Figure 2). Transient voltages couple directly to the comparators, but the input to the sag and surge comparators is first rectified and filtered to obtain the average value of line voltage. Appropriate rms adjustments can be made in software.

The system operates by sampling and resetting the flip-flops every T seconds, where T is the time resolution required in the transient log (perhaps 60 seconds). DACs for the high and low transient levels are set to the desired high and low threshold values. The sag and surge DACs are adjusted after each T-second interval, using a successive-approximation technique to generate high-line and low-line limits that track the current average value.

Assuming a very conservative 1000-instruction routine to perform this successive approximation and the other housekeeping chores, the average CPU performance for T = 60s is 17 instructions per second. The resulting execution rate is 0.00002 MIPS—quite suitable for low-power systems, and far below the 4 MIPS required with an ADC approach. For further power savings the controller can "sleep" most of the time, waking only to process an abnormal line condition. The circuit thus reduces power, complexity, and cost by offloading the voltage comparison from software to analog hardware.

Low-maintenance fault detection and diagnostics

Printer-head control, carriage control, and many other electromechanical applications monitor critical internal voltages and temperatures to determine when to modify their operating mode. In extreme cases, this feedback enables the system to avoid self-destruction by shutting down altogether. For example, a stepper-motor controller must adjust gate drive to the output MOSFETs when necessary to avoid the excessive power dissipation associated with linear operation.

Again, the conventional solution to these monitoring problems is an ADC (**Figure 7a**). The processor directs the ADC to make periodic measurements consistent with the time constant of the process under control. It then scales the resulting digitized values and compares them with limits in software. If they go out of bounds, it can trigger corrective action or shut down the system completely.

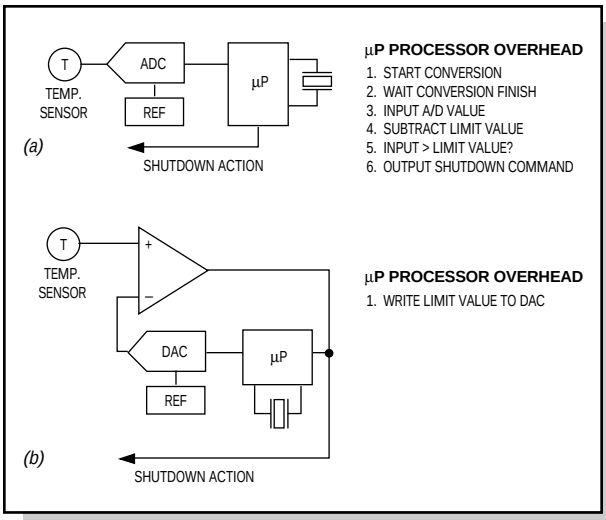


*Figure 7. In this case, replacing an ADC **(a)** with a DAC and comparator **(b)** lowers system cost, response time, and software overhead.*

An alternate approach uses the DAC/comparator combination (**Figure 7b**). The static DAC output establishes a shutdown limit or trip value for the comparator. When a temperature change causes the comparator to trip, the comparator sends an interrupt to the processor that initiates corrective action. If necessary, the processor can also determine the absolute temperature value by initiating a software-based successive-approximation routine.

On the other hand, to support an ADC the processor must poll the ADC, input the sample value, and compare it with the setpoint before jumping to the shutdown routine. Thus, a DAC/comparator not only saves cost and offers a quicker response than does an ADC; it also reduces the processor overhead.

Time-domain reflectometry

Finally, the low cost and low power dissipation of DAC/comparator combinations (vs. ADCs) has made practical the portable time-domain reflectometer (TDR)—an instrument that detects cable discontinuities and measures the intervening transmission length. Portable, inexpensive TDRs have become popular with the proliferation of network cabling.

A TDR operates like radar; it sends a brief pulse along the line and detects any echo returned by an open, short, or other abrupt discontinuity in the line impedance. The time interval for propagation of the outward-bound pulse and its returning reflection is about 3.3ns per foot, assuming a line propagation of 0.6c (six tenths the speed of light). Thus, a 10ns timing resolution in the electronics gives a resolution in distance to the discontinuity of approximately 3 feet.

The ratio of received-pulse amplitude to transmitted-pulse amplitude is used to compute the reflection coefficient. Knowing the reflection coefficient and cable impedance you can compute the impedance of the discontinuity, and from that information deduce the nature of the discontinuity. Coaxial cables introduce a complication by attenuating the pulse on its return trip, so the software must compensate for this effect by applying an amplitude correction based on the distance measurement.

An ADC in this application would have to convert every 5ns (200Msps). Though available, such ADCs are expensive, power hungry, and generally unsuitable for portable applications.

The analog front end of an actual hand-held TDR (**Figure 8**) serves to illustrate the ideas described above. Digital circuitry is excluded for clarity. Though simple and without exotic components, this circuit has impressive performance. It measures termination impedance reliably and with 5% accuracy for cable lengths to 500 feet. For open or shorted terminations, it measures distances to 2000 feet. And best of all, the system (including display and digital circuitry) can operate for 20 hours on a 9V alkaline battery.

The comparator in Figure 8 (IC3) provides single-supply operation with ground sensing and a propagation delay of just 10ns. The DAC (IC4) is a dual device in which one side helps with the pulse-height measurement and the other drives the LCD contrast control (as in Figure 3). Note that the DACs are driven backwards; the (normal) current outputs are driven together by a buffered reference, and the (normal) reference inputs serve as voltage outputs (each buffered by an external op amp).

A simple glitch-monostable circuit (not shown) drives the base of Q1, which in turn drives the cable with positive, 10ns-duration pulses. Any reflections from the line are coupled to the comparator via C3.

IC5 is a bandgap reference whose 1.2V output is buffered by op amp IC2d to provide a reference voltage for the dual DACs in IC4. This reference voltage is also doubled by the gain-of-2 amplifier IC2c to provide a 2.5V dc level at the comparator's noninverting input. DAC A applies 0V to 3.8V at the comparator's inverting input. Levels above 2.5V enable the determination of positive-going pulse heights, and levels below 2.5V determine the amplitude of negative-going pulses.

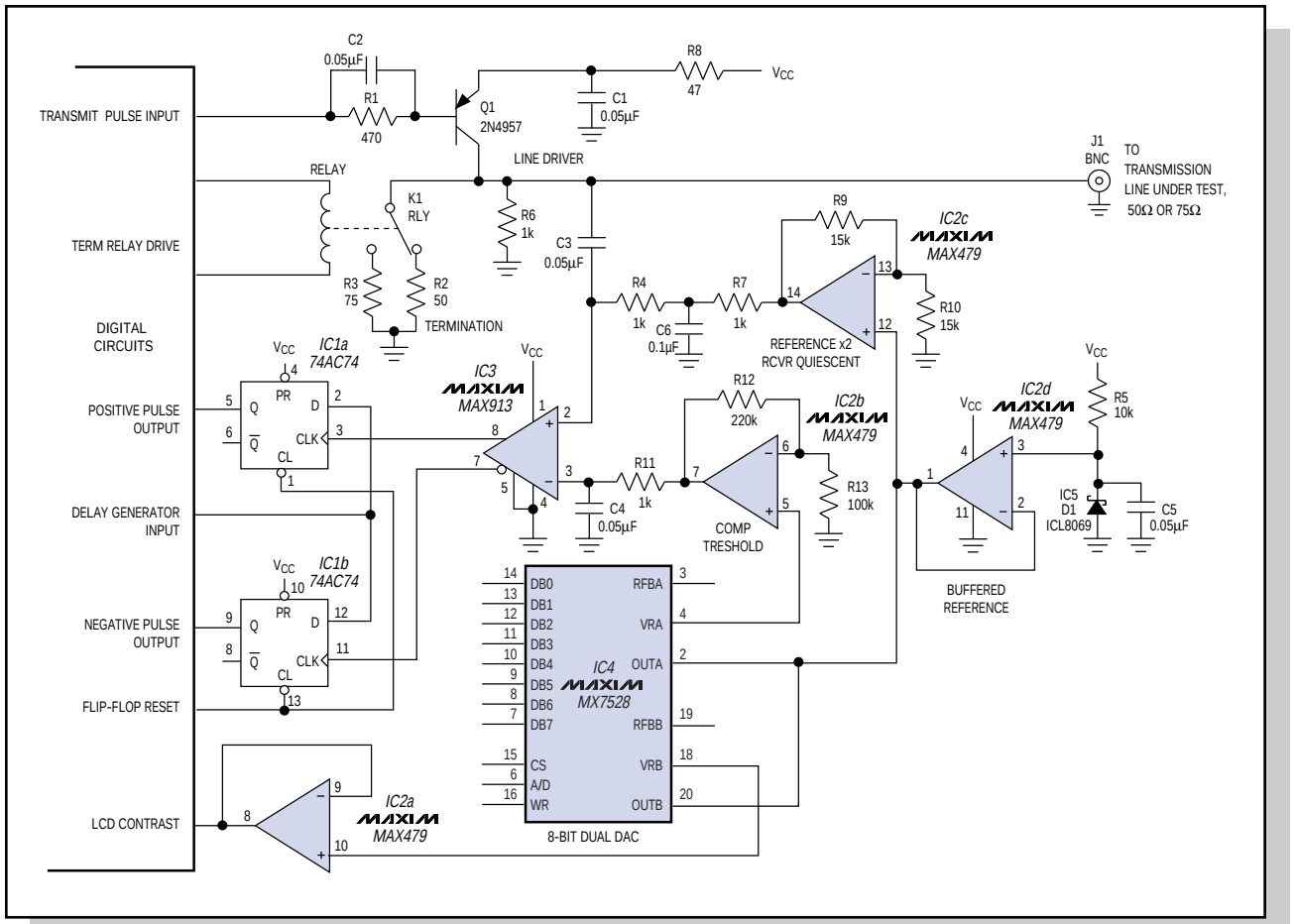


Figure 8. This circuit—the analog section of a time-domain reflectometer—relies on a DAC/comparator in place of an ADC.

Each pulse entering the transmission line also enters a variable delay line in the digital circuitry, which consists of a string of 20ns delay elements controlled by a counter. This delayed pulse from the digital section jointly drives the D inputs of two flip-flops (IC1a and IC1b), which in turn are clocked by complementary TTL outputs from the comparator. Thus, time measurements amount to a race between the return pulse and the pulse going through the delay line: if the D input arrives before a clock transition the flip-flop output is high; otherwise it is zero.

To measure, set the DAC output to a low absolute level and iteratively adjust the delay until the flip-flop output remains at zero, then read the counter. Similarly, to measure the height of return pulses, iteratively adjust the DAC output until the flip-flop output remains at zero, then read the DAC. Note that two flip-flops are required to capture the comparator's leading edge for both positive and negative pulses. This leading edge rises for positive pulses and falls for negative pulses; if both were applied to a single flip-flop, the pulse width would become an unwanted part of the delay.

(Circle 1)

References:

1. Edward Jordan, *Reference Data for Engineers*, 7th Edition, (Howard Sams, 1989).
2. Brian Kenner and John Wettroth, *The Design of a Time-Domain Reflectometer*, (Computer Applications Journal #29, October/November 1992).
3. Paul Horowitz and Winfield Hill, *The Art of Electronics*, 2nd Edition, (Cambridge University Press, 1989).

PC serial port drives 12-bit A/D converter

The **Figure 1** circuit performs a task usually done by a microcontroller—that of driving a 12-bit A/D converter (ADC) from the serial port of a PC. Power consumption is low: the 2mA operating current drops to only 15µA in shutdown.

Interface to the PC is an RS-232 port rather than the transmitter/receiver lines of a UART. The port's Request to Send line (RTS) provides a chip-select signal, and its Data Terminal Ready line (DTR) provides a synchronous-clock signal. A single-supply RS-232 interface chip (IC1) converts these signals from RS-232 levels to CMOS-logic levels (and inverts them in the process). Conversion data appears on the Data Set Ready line (DSR).

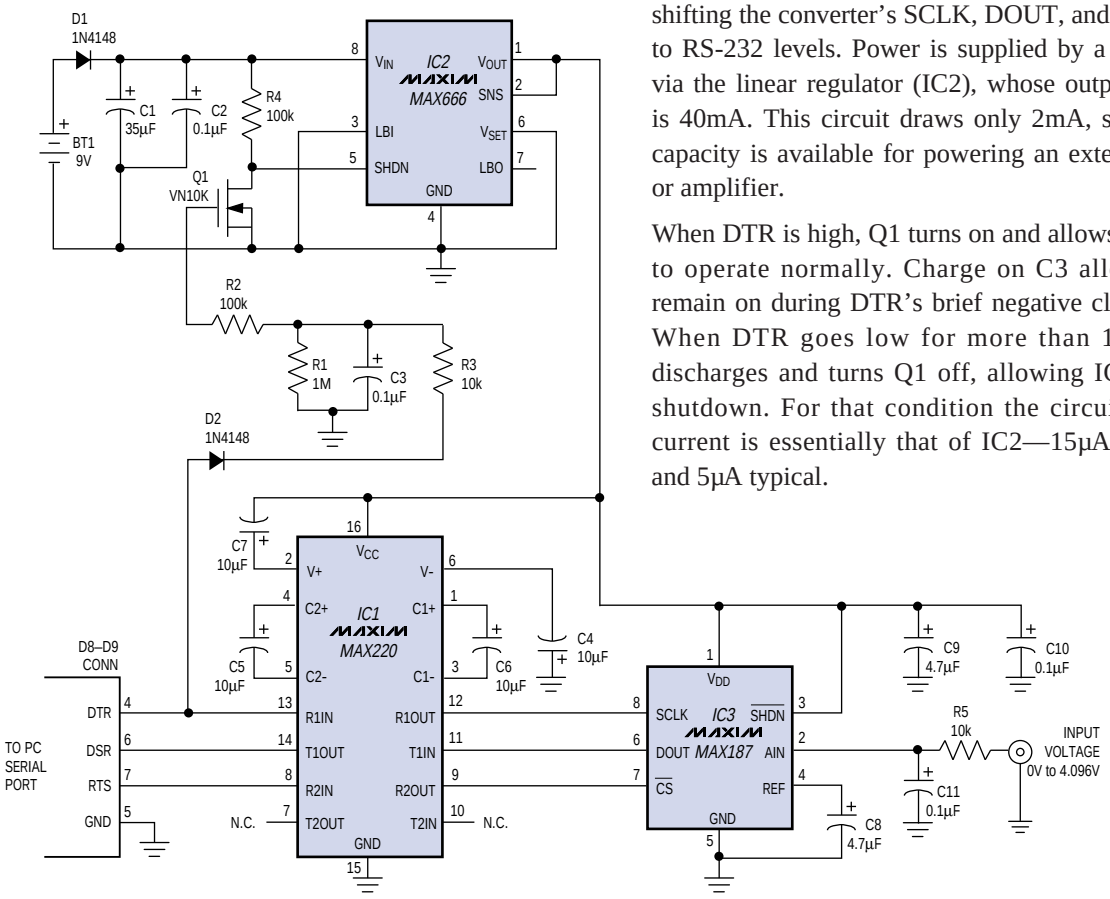


Figure 1. This micropower circuit enables a PC's RS-232 serial port to control a 12-bit A/D converter (IC3).

IC3 is an 8-pin DIP that includes a 12-bit ADC, voltage reference, track/hold, serial interface, and clock generator, plus a 3-wire digital interface consisting of Chip Select ($\overline{CS}$), Serial Clock (SCLK), and Data Out (DOUT). Conversions are initiated by a high-to-low transition on $\overline{CS}$, and take less than 8.5µs. The end of conversion, indicated by a high level on DOUT, leaves the 12-bit result stored in the converter's output shift register. The PC reads this result by clocking DTR while sampling DSR 12 times.

As a low-power version of the venerable (10mA) MAX232, the MAX220 draws only 0.5mA. If power is not a concern, either device is suitable for level-shifting the converter's SCLK, DOUT, and $\overline{CS}$ signals to RS-232 levels. Power is supplied by a 9V battery via the linear regulator (IC2), whose output capacity is 40mA. This circuit draws only 2mA, so the extra capacity is available for powering an external sensor or amplifier.

When DTR is high, Q1 turns on and allows the circuit to operate normally. Charge on C3 allows Q1 to remain on during DTR's brief negative clock pulses. When DTR goes low for more than 100ms, C3 discharges and turns Q1 off, allowing IC2 to enter shutdown. For that condition the circuit's supply current is essentially that of IC2—15µA maximum and 5µA typical.

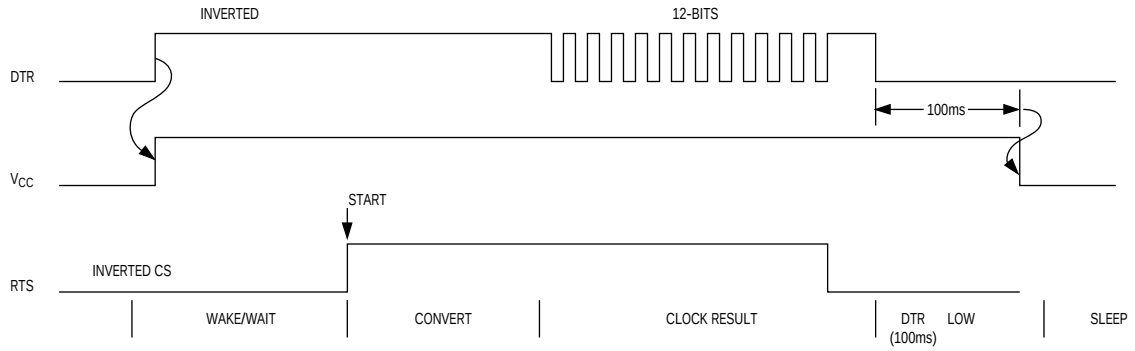


Figure 2. Timing Relationships for Figure 1.

The circuit is controlled by a simple C routine on the PC (request *EJ22 Listing* from Maxim Customer Service). The code drives DTR high to wake the converter, then starts a conversion, waits for completion, clocks out the data, displays the data, and puts the circuit back to sleep. You can then quit by pressing "Q", or trigger another conversion by pressing any key. The software is easily modified for particular applications.

(Circle 2)

PFM control improves dual-output step-up converter

A discrete-component external charge pump enables the PFM-controlled dc-dc converter of **Figure 1** to generate dual outputs with moderate regulation and high efficiency. The circuit accepts input voltages between 2V and 12V (typically 5V) and delivers simultaneous 0mA to 100mA outputs at ±12V (**Figure 2**). Efficiencies range between 80% and 90%.

IC1 regulates 12V via its V+ terminal, but the -12V output has no direct feedback connection. Nevertheless, changes in -12V load current are coupled via "flying capacitor" C1, where they affect the switching frequency just as 12V load changes do—via current-limited, minimum-off-time, pulse-frequency modulation of the chip's internal switching MOSFET. The resulting pseudo-regulation is impressive: a load change of 10mA to 100mA at either output causes only a 4% change in the negative output (from -11.36V to -10.96V).

(Circle 3)

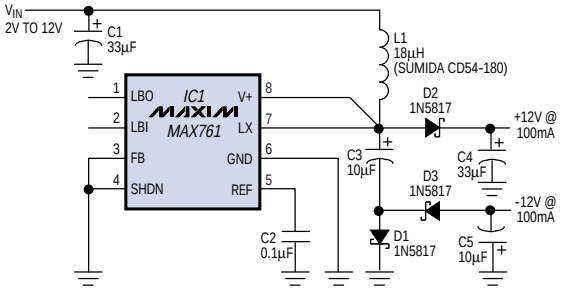


Figure 1. An external charge pump (C3, C5, D1, and D3) enables this dc-dc step-up converter to generate ±12V dual outputs.

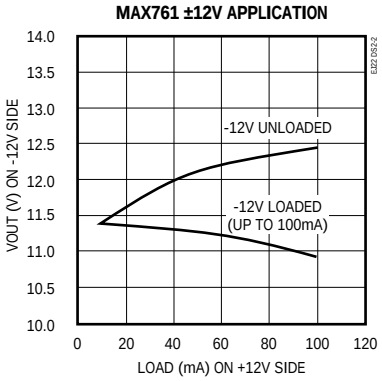


Figure 2. "Pseudoregulation" stabilizes the -12V output in Figure 1.

Synchronous buck-regulator output terminates high-speed data buses

The limitations of today's 5V and 3.3V CMOS buses are causing a proliferation of high-speed, low-voltage buses for the next generation of computers. These new buses—Futurebus, RAMBUS, and GTL (Gunning Transceiver Logic), for example—require low supply rails to reduce signal-voltage swings. Others, such as HSTL and CTT (Center Terminated Transceiver) are also center-terminated and therefore require a power source that can sink current as well as source it.

The termination supply for an HSTL or CTT bus must generate an output of about 0.75V, capable of sourcing and sinking current into a bunch of 50Ω terminating resistors. Designing such supplies can be a headache for two reasons. First, the headroom needed by an emitter-follower pass element in a linear regulator makes it difficult to sink current at such a low voltage. Second, 0.75V is below the magic 1.25V level produced by bandgap circuits as a feedback reference in most linear and switch-mode power-supply ICs.

An efficient, synchronous buck regulator (**Figure 1**) avoids both of these problems. Sink capability at low voltage is accomplished by the use of a synchronous switch (Q2) and by allowing the inductor current to reverse. IC1 includes current-limiting circuitry that prevents inductor-current reversals (as do most buck-regulator ICs), but it also includes a logic input ($\overline{\text{SKIP}}$) that lets you disable that circuitry.

In noise-sensitive wireless applications, pulling $\overline{\text{SKIP}}$ high forces the inductor current to be continuous, thereby avoiding the ringing associated with an otherwise discontinuous inductor current. In this circuit, pulling $\overline{\text{SKIP}}$ high allows current to flow from the circuit output back into the inductor and through the synchronous switch to ground.

The other problem—that of regulating an output level below the 1.25V bandgap threshold—is overcome by dividing down the reference voltage and feeding it to an external integrator amplifier (IC2). Summing this reduced reference with a directly coupled feedback signal ensures an excellent transient response, and produces an integrated feedback signal that feeds directly into the IC's main high-speed PFM comparator.

Current sunk by the output doesn't flow directly to ground as it would in a linear-regulator termination supply. Instead, the buck topology works in reverse and becomes a boost topology, producing a net positive current flow into the 5V supply. In most systems, this excess current is absorbed by the numerous other 5V loads.

(Circle 4)

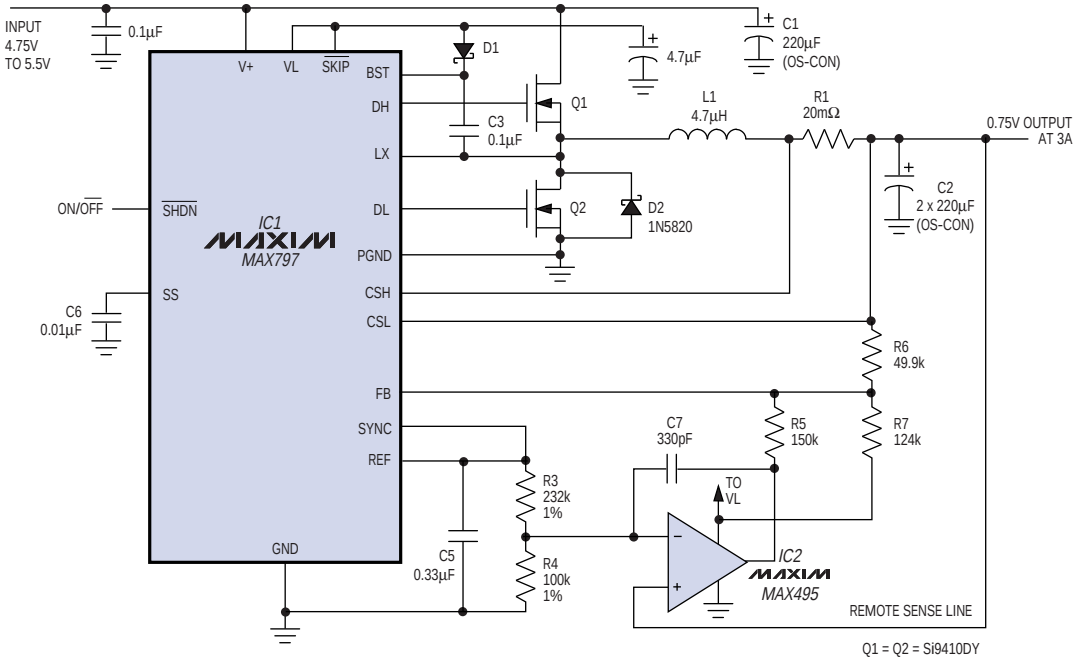


Figure 1. Modifications to a conventional buck-regulator circuit produce a 0.75V, 3A output with sink/source capabilities, useful as a termination supply for high-speed data buses.

Autotransformer regulator inverts 12V to -12V

In **Figure 1**, a dc-dc regulator with internal switching MOSFET inverts 12V to produce an output of 200mA at -12V. The IC is a high-efficiency device whose low quiescent current (120µA maximum) is achieved with a CMOS process that limits the absolute maximum voltage to 21V (input to output). Thus, to avoid 24V across its terminals, the IC must isolate itself from the inductor-flyback voltage by driving either an external switch in a non-boot-strapped configuration, or an internal switch in a flyback-transformer configuration.

Autotransformer T1 (a center-tapped inductor with 1:1 turns ratio) offers a design alternative. In the circuit shown, LX flies back to $\frac{1}{2}V_{OUT}$ plus a diode drop, or approximately -6V. V+ remains at 12V, producing an 18V maximum between V+ and LX that is well within the 21V limit.

Because IC1 drives the gate of its internal MOSFET between the V+ and OUT voltages, you normally connect OUT to V_{OUT} to ensure sufficient gate drive (in a typical application, the chip inverts 5V to -5V). In this circuit the 12V input provides adequate gate drive, so OUT is connected to ground.

(Circle 5)

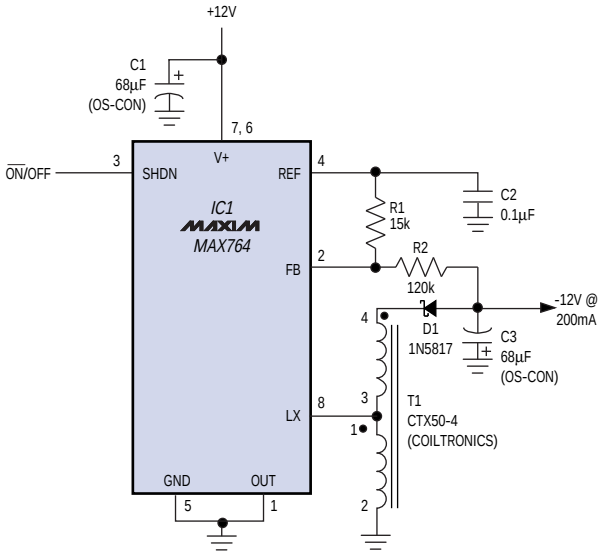


Figure 1. Autotransformer T1 limits the voltage across IC1, allowing use of a high-efficiency chip (with 21V absolute-maximum voltage) in this inverting dc-dc regulator.

Serial-data interface chip supplies bipolar voltages

Some of the interface ICs currently available for serial-data transmission not only operate from low V_{CC} levels (5V or 3.3V); they also generate bipolar dc voltages (±6.5V to ±10V) to support the minimum driver-output levels as specified by EIA/TIA-232. With care, you can steal useful amounts of power from these voltage rails without interfering with the IC's operation.

In **Figure 1**, the IC's switch-mode controller operates with an external inductor, two diodes, and two capacitors to produce ±6.5V. FETs Q1 and Q2 ensure start-up for the circuit by disconnecting the load until these switch-mode supply voltages are present. Note that Q1 must be a logic-level device.

Unlike ICs designed to generate supply voltages, an interface IC generally doesn't specify how much current you can draw from its internally generated supply rails. The amount available depends almost entirely on loads connected to the driver outputs. IC1, for example, guarantees that one transmitter can drive a parallel combination of 3kΩ and 1000pF at 250kbps while the other two maintain dc outputs across 3kΩ loads. These conditions let you calculate the chip's maximum output current capability, but you can't expect to draw extra current while delivering that maximum.

To calculate the maximum output current available, superimpose the ac and dc components: Output current flows alternately from each rail as the NRZ output waveform swings between the guaranteed minimum output levels (±5V). Assuming the output requires one whole data period (4µs at 250kbps) to slew from -5V to +5V, the ac component equals $C_{LOAD}(dv/dt)$ = 1000pF(10V/4µs) = 2.5mA. For the dc component, Ohm's Law gives I = E/R = 5V/3kΩ = 1.67mA from one transmitter, so the three transmitters together represent a dc load of 5mA. Adding the ac and dc components together gives a conservative maximum rating of 2.5mA + 5mA = 7.5mA.

The 3kΩ load is an EIA-232 requirement, but the data rate and load capacitance are application-dependent

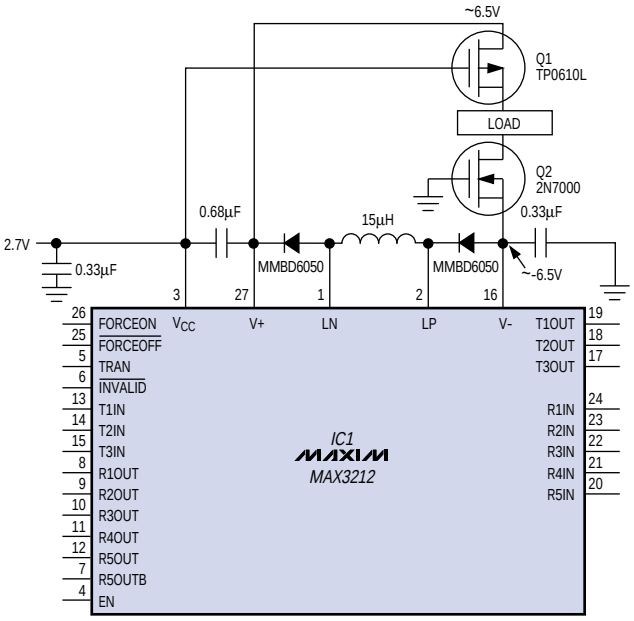


Figure 1. For data rates and driver-output loads less than the maximum allowed, the V+ and V- outputs of this serial-interface IC can supply modest amounts of current to an external circuit.

parameters. Lower values for these parameters make more current available for external use. A remote-sensing system, for instance, might operate at 2400 bits/sec (2400bps) with a load of 3kΩ in parallel with 1000pF (50 feet of cable at 20pF/ft). The dc load for three transmitters is 5mA, and the ac load for one transmitter (72µA) is almost negligible in this low-data-rate application. So, the available current in this case is calculated as 7.5mA - (5mA + 72µA) = 2.428mA.

The above calculation is conservative: with V_{CC} = 2.7V and the three transmitters loaded with 3kΩ||1000pF, a circuit transmitting valid EIA-232 levels at 2400bps will actually deliver 6.7mA to an external load (even more for V_{CC} = 3V and up). As mentioned, Q1 and Q2 enable the circuit to start under these conditions. If you disconnect the transmitter loads, the maximum external load current that allows start-up is 11.5mA. With Q1 and Q2 removed, the maximum is only 5.7mA. **(Circle 6)**

Programmable current source delivers 0A to 5A

The variable current source of **Figure 1** generates 0A to 5A with a compliance range of 4V to 30V. It offers two advantages: the 12-bit D/A converter (IC2) makes it digitally programmable, and the switch-mode step-down regulator (IC1) is more efficient than the alternative current source with linear pass transistor. Applications include battery charging and dc motor control.

IC3 is a high-side, current-sense amplifier normally used in battery-powered systems to detect charge and discharge currents without disturbing the ground path. In this circuit, it senses output current as a voltage drop across R5, and produces a proportional signal current at OUT (pin 8) Thus, the regulator's feedback voltage (pin 1 of IC1) is set by the DAC and modified by IC3's current feedback, which flows across the parallel combination of R2 and R3. This current feedback opposes any change in load current due to a change in load resistance.

The DAC generates 0V to 10V, producing a source current that varies inversely with code: FFF_{HEX} (10V from IC2) produces 0mA, and 000_{HEX} (0V from IC2) produces 5A. For a given programmed level the actual output varies somewhat with load resistance and the corresponding compliance voltage. When tested at 1.5A, for instance, the output of the circuit deviated about +15mA (from 1.5A) for compliance voltages between 10V and 20V (**Figure 2**).

You can reconfigure the circuit for other ranges of output current (I_{SOURCE}) by resizing R2 and R3:

$$I_{SOURCE} = \frac{2217[V_{FB}(R2 + R3) - R3V_{DAC}]}{R2R3},$$

where V_{FB} = 2.21V and V_{DAC} can range from 0V to 10V.

The desired range for I_{SOURCE} defines values for R2 and R3: V_{DAC} = 10V for the low value of I_{SOURCE}, and V_{DAC} = 0V for the high value of I_{SOURCE}. Substituting these two sets of values in the equation yields two equations, to be solved simultaneously for the values of R2 and R3.

(Circle 7)

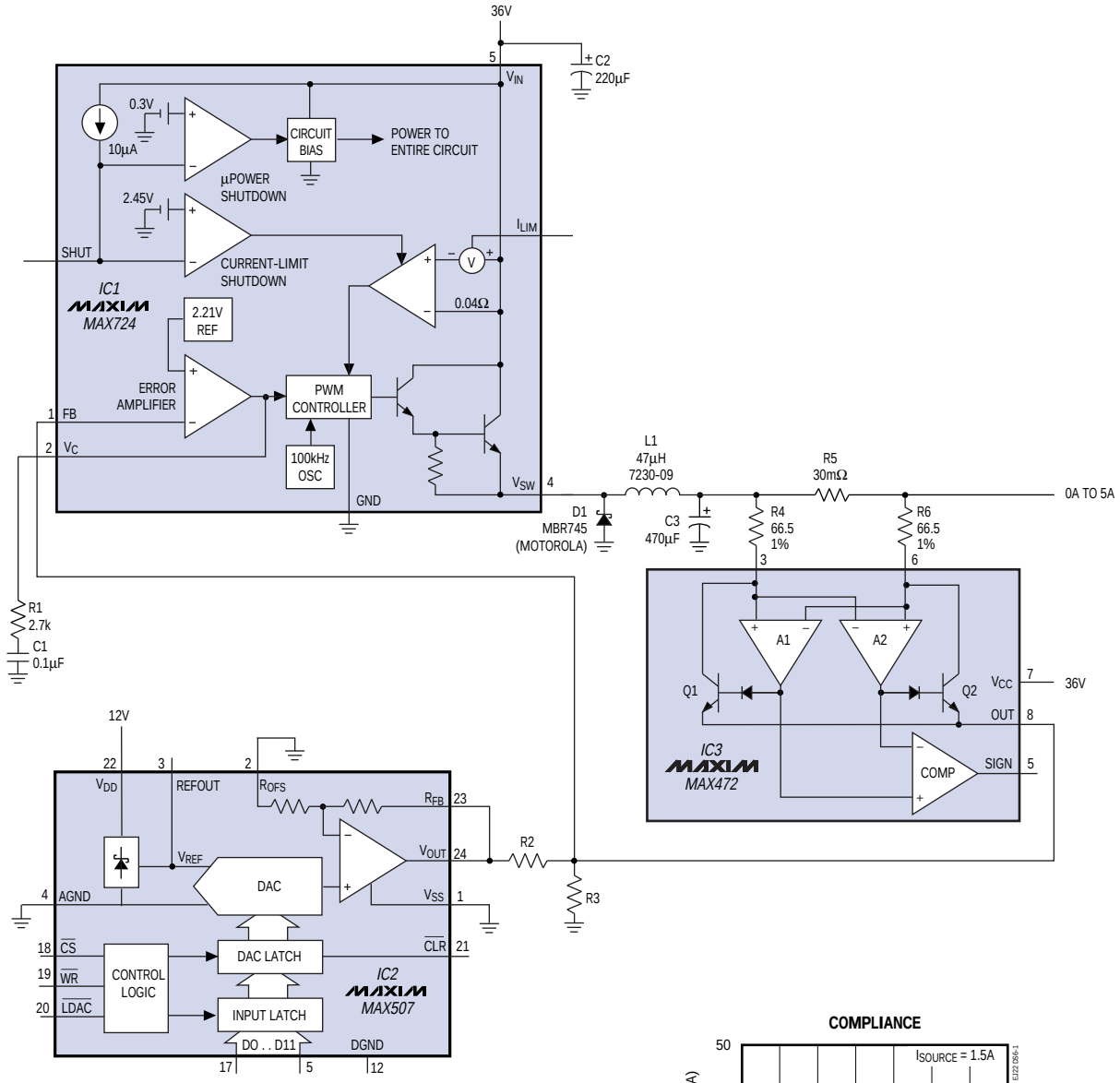


Figure 1. This programmable current source generates 0A to 5A, with 12-bit resolution and a compliance range of 4V to 30V.

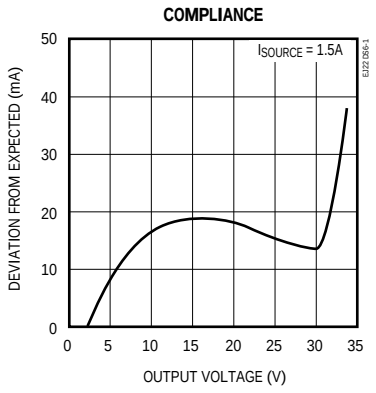


Figure 2. For a programmed level of 1.5A, the output current in Figure 1 deviates with output (compliance) voltage as shown.

NEW PRODUCTS

Ultra-low-power, open-drain, comparator-plus-reference ICs draw only 4µA

The MAX971–MAX974 and MAX981–MAX984 single/dual/quad comparator-plus-reference families offer the lowest power consumption available: less than 4µA over the extended temperature range for MAX971, MAX972, and MAX981 devices operating with a 5V supply. All devices operate from 2.5V to 11V, or with dual supplies of ±1.25V to ±5.5V. Input voltages may range from the negative supply rail to within 1.3V of the positive rail.

All but the MAX972 include 1.182V bandgap references: the MAX971/MAX973/MAX974 have ±1% references, and the MAX981–MAX984 have ±2% references. Further, the MAX983 (hardwired for window-detector applications) and the MAX971/MAX973/MAX981/MAX982 let you add hysteresis without recourse to feedback or complicated equations—by connecting two external resistors to the HYST input. The resulting hysteresis is independent of supply voltage and has no effect on high-Z inputs.

Open-drain outputs enable all comparators to implement wire-OR configurations. By giving access to the output transistor's source terminal (GND) as well, the MAX971/MAX974/MAX981/MAX984 devices easily implement level translators and bipolar to single-ended converters. For standard complementary CMOS output stages, consider these otherwise-similar families: MAX921–MAX924 (with ±1% references) and MAX931–MAX934 (with ±2% references).

MAX974 and MAX984 devices come in 16-pin DIP and narrow SO packages; all others come in 8-pin DIP, SO, and µMAX packages. The MAX98x family offers versions tested for the commercial (0°C to +70°C) and extended-industrial (-40°C to +85°C) temperature ranges; the MAX97x family offers military (-55°C to +125°C) versions as well. **(Circle 8)**

DEVICE	INTER. REF	INTER. HYST	PRICE $†
MAX971 Single	1%	Yes	1.50
MAX972 Dual	None	No	0.98
MAX973 Dual	1%	Yes	1.95
MAX974 Quad	1%	No	2.25
MAX981 Single	2%	Yes	0.98
MAX982 Dual	2%	Yes	1.26
MAX983 Dual	2%	Yes	1.26
MAX984 Quad	2%	No	1.31

† 1000 up, FOB USA

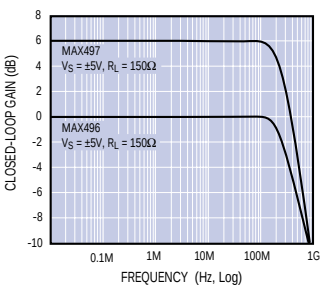
275MHz quad video buffers drive 50Ω and 75Ω cables

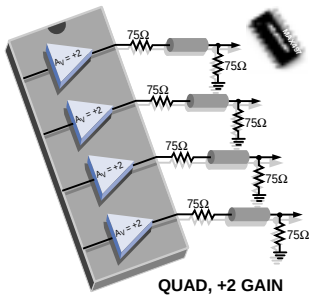
The MAX496 and MAX497 are closed-loop, quad video buffers optimized for driving 50Ω and 75Ω back-terminated cables directly. The MAX496 has a fixed gain of 1V/V (0dB), and the MAX497 has a fixed gain of 2V/V (6dB). The MAX496 features a 1550V/µs slew rate and a small-signal, -3dB bandwidth of 375MHz; the MAX497 features a 1450V/µs slew rate and a small-signal, -3dB bandwidth of 275MHz. Along with low differential gain and phase errors (0.01% and 0.01°), this high-speed performance suits the buffers for broadcast-quality composite video, all component-video applications (multimedia, medical imaging graphics), and general high-speed signal processing.

MAX496/MAX497 buffers operate on ±5V and draw only 8mA (typical) per channel. Gain flatness to within ±0.1dB extends to 80MHz for the MAX496 and to 120MHz for the MAX497. High-speed performance is maximized by low channel input capacitance (2pF), which lets MAX496/MAX497 buffers settle to 0.1% in only 14ns. To further minimize crosstalk and simplify board layout, the input channels are located on non-adjacent package pins.

Available in 16-pin plastic DIP and narrow-SO packages, the MAX496 and MAX497 are screened for the commercial (0°C to +70°C) temperature range. Prices start at $4.95 (1000 up, FOB USA).

(Circle 10)





QUAD, +2 GAIN

350MHz voltage-feedback op amp has 1300V/µs slew rate

The MAX477 is a fast, unity-gain-stable op amp whose standard voltage-feedback topology allows all the gain configurations common to general-purpose op amps. Its unique input stage, however, lets it combine the advantages of current feedback (high slew rate and a large full-power bandwidth) with those of voltage feedback (low input offset voltage, low input bias current, low current and voltage noise, and two high-impedance inputs).

The MAX477 has a fast slew rate of 1300V/µs and is ideally suited for driving 50Ω and 75Ω loads. At unity gain, it has a small-signal bandwidth of 350MHz and a full-power bandwidth of 170MHz.

In addition to high speed, the MAX477's precision makes it suitable for use in broadcast and high-definition TV systems, in video switching and routing applications, and as a preamplifier for flash A/D converters. Precision specifications include 2µA input bias current, 65dB open-loop gain, 0.1dB gain flatness to 100MHz, low differential phase/gain errors of 0.01°/0.01%, and voltage/current noise densities of 5nV/√Hz and 2pA/√Hz, respectively.

The MAX477 comes in 8-pin DIP, SO, and µMAX packages, in versions tested for the extended-industrial (-40°C to +85°C) and military (-55°C to +125°C) temperature ranges. Prices start at $2.40 (1000 up, FOB USA). **(Circle 9)**

NEW PRODUCTS

Op-amp family provides low noise and ultra-low distortion

MAX4106–MAX4109 op amps constitute a new family of high-speed, voltage-feedback devices that are unprecedented for their low levels of distortion and noise. Available in 8-pin SO packages, they operate on ±5V and deliver up to 90mA from ±3.5V output swings.

The MAX4106/MAX4107 are useful in ultra-low-noise ADC preamps, ultrasound applications, and high-performance receivers. Their compensation for closed-loop gain yields a minimum of 5V/V for the MAX4106 and 10V/V for the MAX4107. They combine high speed (350MHz for the MAX4106, 300MHz for the MAX4107) with very low voltage noise (0.75nV/√Hz). Their spurious-free dynamic range (SFDR) at 5MHz, with V_{OUT} = 2Vp-p, is -63dBc for the MAX4106 (at 5V/V) and -60dBc for the MAX4107 (at 10V/V). Slew rates are 275V/µs (MAX4106) and 500V/µs (MAX4107).

The MAX4108/MAX4109 op amps combine high speed with extremely low distortion, making them suitable for use in RGB and composite video, ADC preamps, and high-performance RF signal processing. The unity-gain-stable MAX4108 has a 20MHz SFDR of -81dBc and a unity-gain bandwidth of 400MHz. The MAX4109 (stable for A_{VCL} = 2V/V or more) has a 20MHz SFDR of -80dBc and a -3dB bandwidth of 225MHz. Both have 1200V/µs slew rates. For V_{OUT} = 2Vp-p, the full-power bandwidths are 300MHz (MAX4108) and 200MHz (MAX4109).

The MAX4106/MAX4107 come in 8-pin SO packages, and the MAX4108/MAX4109 come in 8-pin SO and µMAX packages. All are tested for the extended-industrial (-40°C to +85°C) temperature range. Prices start at $3.88 (1000 up, FOB USA).

(Circle 11)

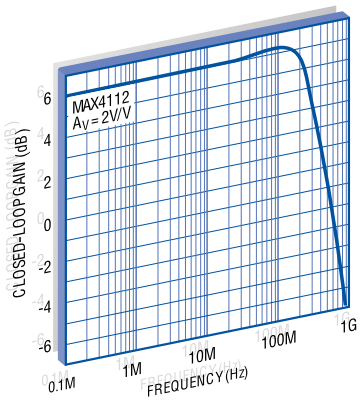
500MHz, current-feedback video amplifiers draw 5mA and deliver 80mA out

The MAX4112 and MAX4113 video amplifiers employ current-mode feedback to achieve very high slew rates and gain-bandwidth products. The MAX4112, stable for closed-loop gains (A_{VCL}) of two or more, slews at 1200V/µs and has a -3dB bandwidth of 500MHz at A_{VCL} = 2. Its full-power bandwidth is 300MHz at V_{OUT} = 2Vp-p.

The MAX4113 has a -3dB bandwidth of 275MHz and is stable for A_{VCL} = 8 or more. Its full-power bandwidth at V_{OUT} = 2Vp-p is 250MHz, and its slew rate is 1800V/µs. Both devices specify 0.01°/0.01% for differential phase and gain error, and both are well suited for high-performance pulse, RF, and video applications.

MAX4112/MAX4113 op amps come in 8-pin SO packages, tested for the extended-industrial (-40°C to +85°C) temperature range. Prices start at $1.95 (1000 up, FOB USA).

(Circle 12)



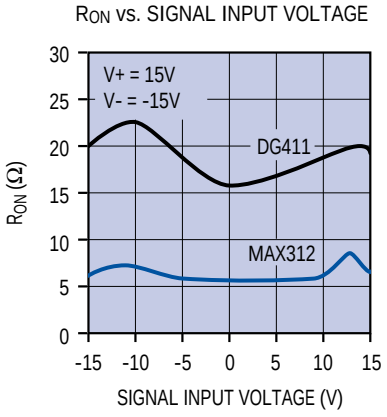
Quad, SPST analog switches offer 10Ω on-resistance

The MAX312/MAX313/MAX314 are quad, single-pole/single-throw analog switches with low R_{ON} (10Ω max), R_{ON} variations no greater than 2Ω over the specified signal range, and tight matching between channels (1.5Ω max). MAX312 switches are normally closed (NC), MAX313 switches are normally open (NO), and the MAX314 has two NC and two NO switches.

Each device operates on single (4.5V to 30V) or dual (±4.5V to ±20V) power supplies, handles rail-to-rail signals, conducts equally well in both directions, and exhibits leakages of no more than 2.5nA at +85°C. Pin compatible with DG411/DG412/DG413 devices, the MAX312/MAX313/MAX314 guarantee ESD protection greater than 2000V, per Method 3015.7 of MIL-STD-883. Crosstalk at 20kHz is greater than 96dB.

MAX312/MAX313/MAX314 switches come in 16-pin DIP and narrow-SO packages, in versions tested for the commercial (0°C to +70°C), extended-industrial (-40°C to +85°C), and military (-55°C to +125°C) temperature ranges. Prices start at $2.49 (1000 up, FOB USA).

(Circle 13)



NEW PRODUCTS

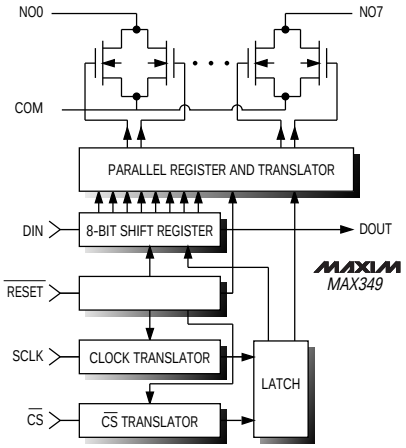
8-channel and dual 4-channel multiplexers have serial control

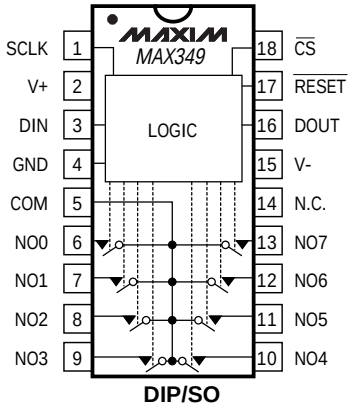
The MAX349 and MAX350 multiplexers (8-channel and dual 4-channel) offer serially controlled channel selection. On-resistances are 100Ω maximum, matched to within 16Ω max between switches and flat to within 10Ω max over the specified signal range. All channels conduct equally well in either direction.

Each CMOS device operates with a ±2.7V to ±8V dual supply or a 2.7V to 16V single supply. Each handles rail-to-rail input signals, and exhibits an off-leakage current of only 0.1nA at +25°C (5nA at +85°C). At power-up, an automatic reset opens all switches and fills all internal shift registers with zeros. Each IC also provides an asynchronous $\overline{\text{RESET}}$ input.

The serial interface is compatible with the SPI™, QSPI™, and Microwire™ synchronous-serial standards. Functioning as a shift register, it synchronously clocks in data (at DIN) with the rising edge of the clock (SCLK). The shift-register output (DOUT) lets you connect several MAX349s or MAX350s together in a daisy-chain configuration. Because all digital inputs have 0.8V and 2.4V logic thresholds, the ICs ensure compatibility with TTL and CMOS logic when operating with 5V or ±5V supplies.

MAX349/MAX350 multiplexers are available in 18-pin DIP, 18-pin wide-SO, and 20-pin SSOP packages, in versions tested for the commercial (0°C to +70°C), extended-industrial (-40°C to +85°C), and military (-55°C to +125°C) temperature ranges. Prices start at $2.98 (1000 up, FOB USA). **(Circle 14)**





DIP/SO

SPI and QSPI are trademarks of Motorola, Inc.
Microwire is a trademark of National Semiconductor Corp.

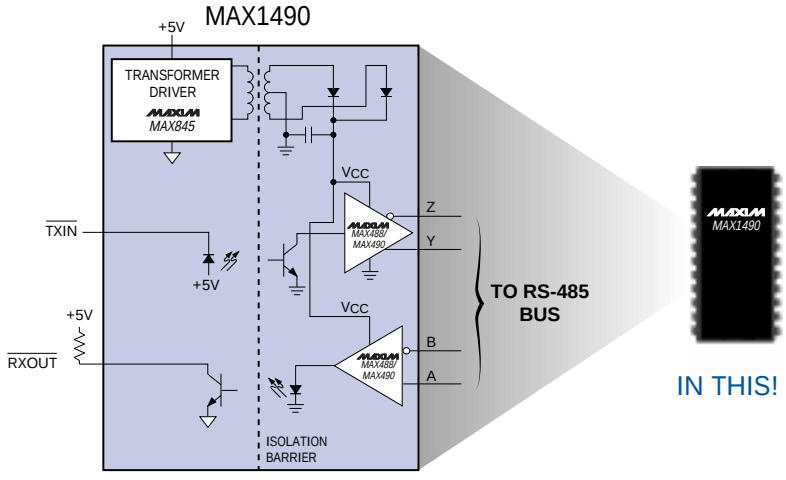
Complete, isolated, full-duplex RS-485/ RS-422 interface costs under $10

The MAX1490A/MAX1490B full-duplex data-communications transceivers provide an electrically isolated RS-485 or RS-422 interface in a single package. Each fully isolated transceiver operates from a single 5V supply on the other (logic) side of the isolation barrier, and the entire circuit—including transceiver ICs, opto-couplers, and transformer—fits in a 24-pin DIP. The isolation barriers typically withstand 1600V_{rms} for one minute or 2000V_{rms} for one second.

The MAX1490A handles data rates as high as 2.5Mbps. The MAX1490B, which provides error-free transmissions to 250kbps, has slew-rate-limited drivers that minimize electromagnetic interference (EMI) while reducing any reflections caused by improperly terminated cables.

Each driver output has short-circuit current limiting and thermal-shutdown circuitry, which prevents excessive power dissipation by placing the outputs in a high-impedance state. Each input and output meets all RS-485 and RS-422 specifications. As a fail-safe feature in response to an open-circuited input, the receivers guarantee a logic-high output state for RO. (The MAX1480A/MAX1480B are similar products, but offer half-duplex operation.)

The transceivers come in 24-pin wide plastic DIPs, tested for the commercial (0°C to +70°C) and extended-industrial (-40°C to +85°C) temperature ranges. Prices start at $10.98 for the MAX1490A and at $10.50 for the MAX1490B (1000 up, FOB USA). **(Circle 15)**



ALL THIS... IN THIS!

NEW PRODUCTS

Low-voltage, quad, SPST analog switches offer low cost

MAX4066 and MAX4066A analog switches are designed to outperform the pin-compatible, industry-standard 74HC4066 types. MAX4066A switches (unlike 74HC types) offer guaranteed limits for on-resistance (45Ω with 12V supply), R_{ON} matching between channels (2Ω max), and leakage (100pA max at +25°C). For even lower cost, the MAX4066 offers 45Ω max R_{ON} and a 4Ω match (with a 12V supply). MAX4066 leakage is 1nA max at +25°C.

Fully specified at 3V, 5V, and 12V, the MAX4066/MAX4066A switches guarantee operation for supply voltages from 2V to 16V. At 12V, for example, both offer 45Ω maximum on-resistance, 2Ω channel-to-channel matching, and 4Ω flatness over the specified signal range. Input signals range from V+ to ground, inclusive.

Each device is suitable for application as a multiplexer, demultiplexer, or bilateral switch. Channel selection is by applied TTL/CMOS logic levels. Low off-leakage (100pA max for the MAX4066A) and low power consumption (0.5µW) make MAX4066/MAX4066A switches ideal for battery-operated applications. Each offers ESD protection beyond 2000V, per Method 3015.7 of MIL-STD-883.

MAX4066/MAX4066A devices come in 14-pin DIPs, narrow-SO packages, and a 16-pin QSOP, in versions tested for the commercial (0°C to +70°C), extended-industrial (-40°C to +85°C), and military (-55°C to +125°C) temperature ranges. Prices start at $0.99 for the MAX4066 and at $1.87 for the MAX4066A (1000 up, FOB USA). **(Circle 16)**

Ultra-thin PCMCIA power supplies fit Type 1 and Type 2 cards

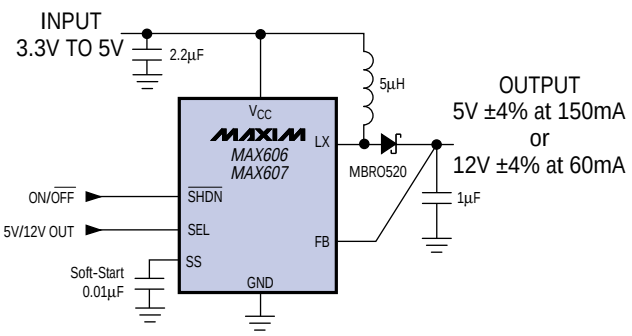
1MHz, 1.25mm-high boost converters occupy only 0.25in²

MAX606/MAX607 dc-dc converters require less height and less pc area than any other equivalent ICs. Intended for Type 1 and Type 2 PCMCIA cards and other low-profile applications, they stand only 1.11mm high in the 8-pin µMAX package. Their high switching frequency (to 1.2MHz for the MAX606) enables the use of small external components that yield 1.35mm-high Type-1 circuits only 0.25in² in area, and slightly taller Type-2 circuits only 0.16in² in area.

MAX606/MAX607 devices accept input voltages between 3V and 5.5V, and produce regulated outputs of 5V or 12V according to the state of an applied logic signal. With two external resistors you can adjust the output to any level between V_{IN} and 12.5V. Output accuracy is guaranteed ±4%. For load currents between 2mA and 200mA, the converters' current-limited pulse-frequency-modulated (PFM) control scheme produces efficiencies between 80% and 90%. The output current is 60mA at 12V (guaranteed) or 120mA at 5V.

The MAX606 switching frequency (double that of the MAX607) ranges from 600kHz to 1.2MHz, depending on the input and output voltages and other operating conditions. Thus, the lower-frequency MAX607 circuits require somewhat larger external components. Both devices have a logic-controlled shutdown mode that saves battery life by reducing supply current to 1µA. At power-up, a user-set soft-start circuit prevents input surge currents.

A preassembled, Type-1 evaluation kit (MAX606EVKIT-MM) is available to speed MAX606 designs. The MAX606 and MAX607 are available in 8-pin µMAX and SOIC packages, tested for the extended-industrial (-40°C to +85°C) temperature range. Prices start at $3.25 (1000 up, FOB USA). **(Circle 17)**



Step-up controller generates fixed (5V) or adjustable (3V to 16.5V) outputs

The MAX608 is a low-voltage step-up controller that operates from a 1.8V to 16.5V input. Its output voltage is either fixed at 5V or (with an external resistor divider) variable from 3V to 16.5V. No-load operating current is only 85µA, or 2µA (5µA max) in the shutdown mode. For heavy loads, the regulator's current-limited PFM control scheme (pulse-frequency modulation) ensures high 85% efficiency from 30mA to 1.5A.

The MAX608 controller is an excellent choice for 2-cell and 3-cell battery-powered systems. Its high operating frequency (to 300kHz) allows the use of small, surface-mount external components. The MAX608 operates only in "bootstrapped" mode, with its output voltage connected to its supply terminal (OUT). For a 12V output or for non-bootstrapped applications—in which the chip is powered by the input voltage—refer to the pin-compatible MAX1771.

An evaluation kit for the MAX608 is available as a design aid from Maxim. MAX608s come in 8-pin plastic DIP or SO packages, in versions tested for the commercial (0°C to +70°C) and extended-industrial (-40°C to +85°C) temperature ranges. Prices start at $1.89 (1000 up, FOB USA).

(Circle 18)

NEW PRODUCTS

Low-voltage, 8-channel SPST switch has serial interface

The MAX395 includes eight independent, separately controlled single-pole/single-throw (SPST) switches in a 24-pin package. Conducting equally well in either direction, the switches guarantee on-resistances of 100Ω. R_{ON} is matched to within 5Ω max between switches and flat to within 10Ω over the specified signal range. Off leakages are only 0.1nA at +25°C (10nA at +25°C).

A CMOS device, the MAX395 operates with dual supply voltages of ±2.7V to ±8V, or a single supply voltage in the 2.7V to 16V range. For 5V or ±5V supplies, the digital inputs' guaranteed logic thresholds (0.8V and 2.4V) ensure TTL/CMOS compatibility. Each switch can handle rail-to-rail analog voltages. The MAX395's pinout is compatible with the industry-standard MAX335 octal analog switch.

The MAX395 serial interface is compatible with the SPI™, QSPI™, and Microwire™ synchronous-serial standards. Functioning as a shift register, it lets you clock in data (at DIN) synchronously with the rising edges of CLK. Then, a rising edge at $\overline{CS}$ transfers data to the switches, affecting them simultaneously. The shift-register output (DOUT) lets you cascade several MAX395 devices in a daisy-chain configuration.

At power-up, an automatic reset ensures that all switches are open and the internal shift registers are cleared to zero. In addition, the $\overline{RESET}$ input lets the MAX395 respond to asynchronous reset commands. ESD (electrostatic discharge) protection is rated at greater than 2kV per Method 3015.7 of MIL-STD-883.

The MAX395 comes in a 24-pin narrow DIP or wide-SO package, in versions tested for the commercial (0°C to +70°C), extended-industrial (-40°C to +85°C), and military (-55°C to +125°C) temperature ranges. Prices start at $2.98 (1000 up, FOB USA).

(Circle 19)

Low-power, slew-rate-limited RS-485/RS-422 transceivers are ESD protected to ±15kV

The low-power transceivers MAX481E, MAX483E, MAX485E, MAX487E–MAX491E, and MAX1487E are intended for RS-485 and RS-422 communications in harsh environments. Each device contains one driver and one receiver, for which the driver output and receiver input are protected to ±15kV against electrostatic discharge (ESD) simulated by the Human Body Model. Further, the chips guarantee freedom from latchup in the presence of ESD.

Drivers in the MAX481E, MAX485E, MAX490E, MAX491E, and MAX1487E allow data transmissions to 2.5Mbps. Drivers in the MAX483E, MAX487E, MAX488E, and MAX489E have reduced slew rates that minimize EMI (electromagnetic interference) and the reflections caused by improperly terminated cables. As a result, these transceivers can produce error-free data transmissions to 250kbps. Common-mode input ranges are -7V to 12V.

All transceivers operate from 5V. When unloaded or when fully loaded with disabled drivers, the MAX488E and MAX489E draw supply currents as low as 120µA. MAX481E, MAX483E, and MAX487E transceivers each have a shutdown mode that lowers supply current to only 0.5µA. All driver outputs are current-limited for protection against short circuits. For protection against excessive power dissipation, all drivers include thermal-protection circuitry that drives the output to a high-impedance state when required. All receivers include fail-safe circuitry that guarantees logic-high outputs in the presence of open-circuited inputs.

MAX488E–MAX491E devices are designed for full-duplex communications; MAX481E, MAX483E, MAX485E, MAX487E, and MAX1487E devices are designed for half-duplex communications. For the MAX487E and MAX1487E, receiver input impedances of ¼-unit load allow as many as 128 transceivers on an RS-485 or RS-422 bus. (By comparison, these buses support only 32 standard transceivers.) For applications that are not ESD sensitive, use the economical "non-E" transceivers: MAX481, MAX483, MAX485, MAX487–MAX491, and MAX1487.

The MAX489E and MAX491E come in 14-pin plastic DIP and SO packages; all others come in 8-pin plastic DIP and SO packages. All are available in versions tested for the commercial (0°C to +70°C) and extended-industrial (-40°C to +85°C) temperature ranges. The MAX1487E is also available in a military version (-55°C to +125°C). Prices start at $1.50 (1000 up, FOB USA).

(Circle 21)

Lowest-dropout SOT-23 linear regulators deliver 50mA

MAX8863* and MAX8864* linear regulators are designed primarily for battery-powered applications. Operating from inputs in the 2.5V to 5.5V range, they deliver output currents as high as 50mA with a maximum dropout voltage of 120mV. PMOS pass transistors ensure that the low 80µA supply current remains independent of load current, making the MAX8863/MAX8864 regulators suitable for use in modems, cellular and cordless telephones, and other portable equipment.

Each device features Dual Mode™ operation, which offers the option of a fixed or adjustable output voltage: MAX8863T/ MAX8864T regulators are preset at 3.175V, and MAX8863S/ MAX8864S regulators are preset at 2.850V. Both versions let you set their output in the range 1.25V to 5.5V with an external resistor divider.

These regulators have a shutdown mode that lowers their supply current to 0.1µA. Shutdown causes the MAX8864 to actively discharge its output voltage to ground, but the devices are otherwise identical. Common features include short-circuit protection, thermal-shutdown protection, and reverse-battery protection.

MAX8863/MAX8864 regulators come in a 5-pin SOT-23 package, screened for the extended-industrial temperature range (-40°C to +85°C). **(Circle 20)**

** Future product—contact factory for availability.*
Dual Mode is a trademark of Maxim Integrated Products.