Hardware Technologies for Robust Personal Communication Transceivers

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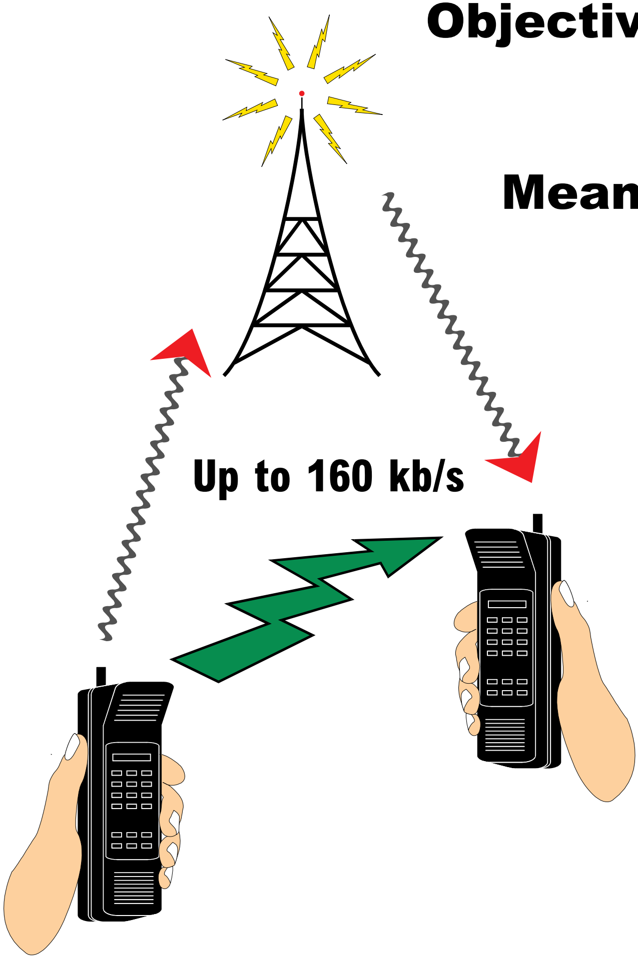
UCLA Low-Power Transceiver Program

Objective: Low-power, handheld, robust transceivers for indoor and mobile personal communications

Means: Investigate analog, digital, and antenna technologies, coupled tightly to system design



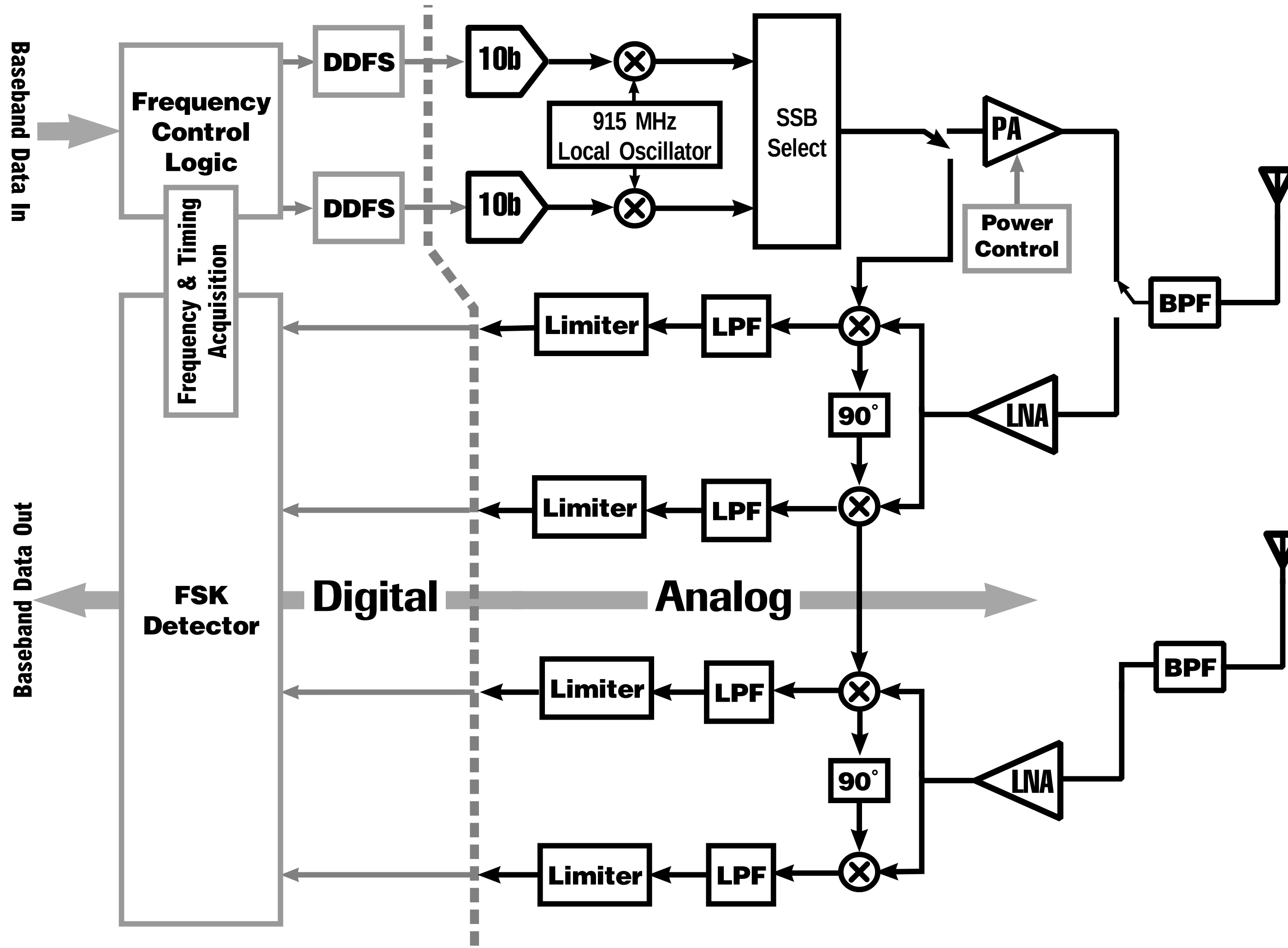
Robustness

- Space Diversity with Multiple Antennas
- Frequency Diversity with Spread-Spectrum
- Time Diversity with ECC/Interleaving

Low Power Dissipation

- Low-Voltage Custom Analog & Digital CMOS
- Monolithic CMOS 915 MHz Receive/Transmit Path
- Two-chip Design; Minimum Discrete Components

The UCLA Frequency-Hopped Spread-Spectrum CMOS Transceiver



Performance Specifications of Handset

Power Dissipation of Handset	225 mW in receive, 300 mW in transmit
Frequency Band	902-928 MHz (unlicensed ISM band)
Radiated Power	20 mW (max); 20 μW (min)
Data Rate	2 to 160 kb/s (variable)
Duplexing	Time Division Duplex between TX and RX
Multiple Access Method	Frequency-Hopped Spread-Spectrum CDMA
Coding	Rate-½ Convolutional Code (k=6)
Modulation	Binary or Quaternary FSK
Power Supply	3 V (max)
IC Technology	1-μm bulk CMOS
Receive Antennas	Multiple miniature embedded elements with space and polarization diversity

Spread-Spectrum Systems: Hardware Implications

Direct Sequence

- Frequency Diversity by making chip-rate >> symbol rate
- Equalization at *chip-rate* ➪ High-speed signal processing required
- Coherent receiver most common
- Main advantage: SNR gain with coherent detection, optimum modulation
- Limitation: High complexity

Frequency Hopped

- Covers wide bandwidth with low hop-rate
- Equalization at *hop-rate* only
- Simple binary FSK modulation may be used
- Non-coherent receiver is simple
- Main advantage: Low-power receiver
- Limitation: Sub-optimal channel capacity

Diversity Techniques

☞ Multiple Antennas

- Antennas receive uncorrelated signals
- Use space and polarization diversity

☞ Frequency Spreading

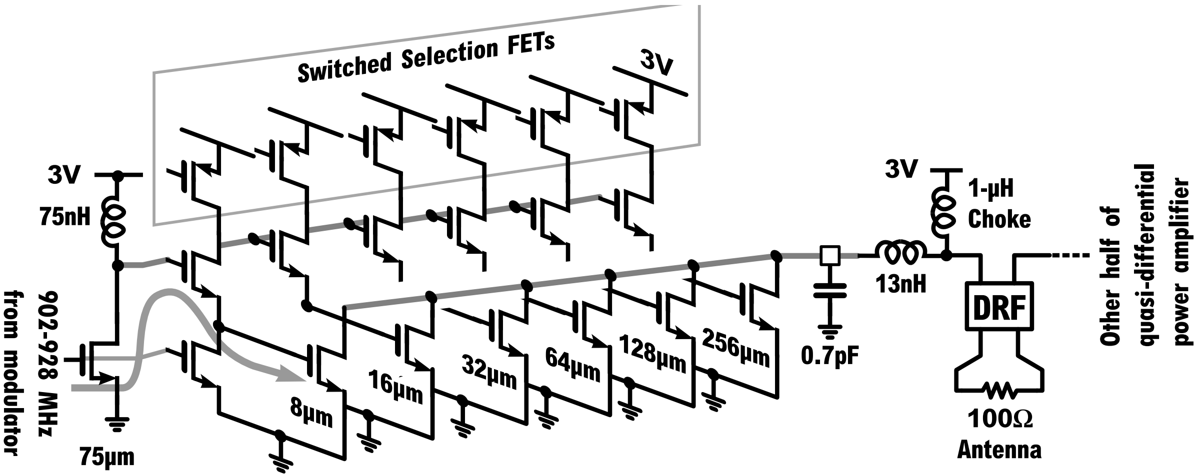
- Code-Division Multiple Access (CDMA); Direct Sequence OR Frequency Hop
- Time-Division Multiple Access (TDMA); Equalization

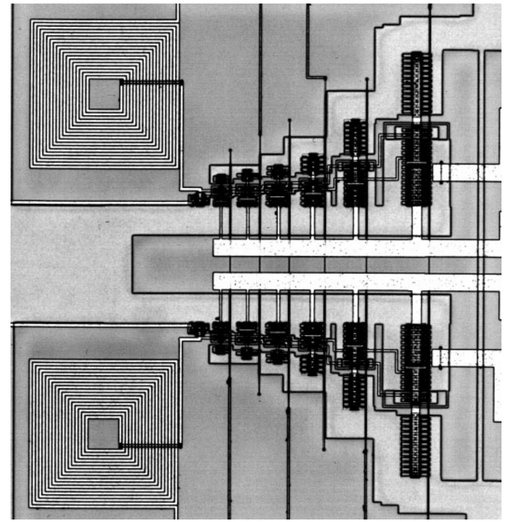
☞ Time Diversity

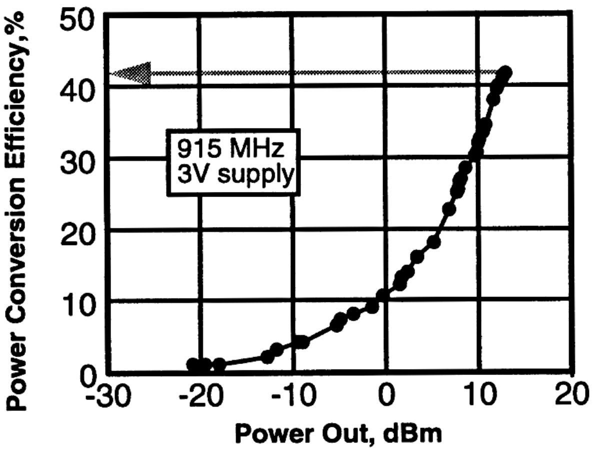
- Coding
- Interleaving

☞ Power Control

Power Amplifier

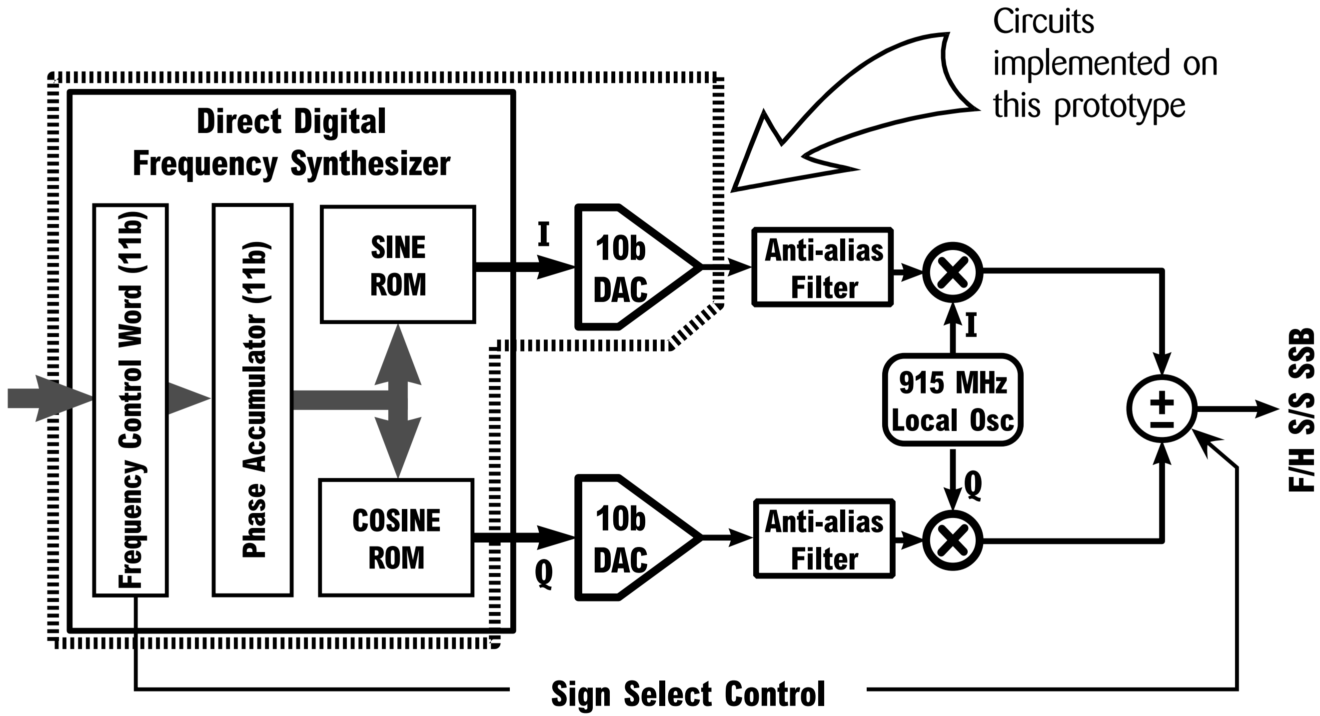






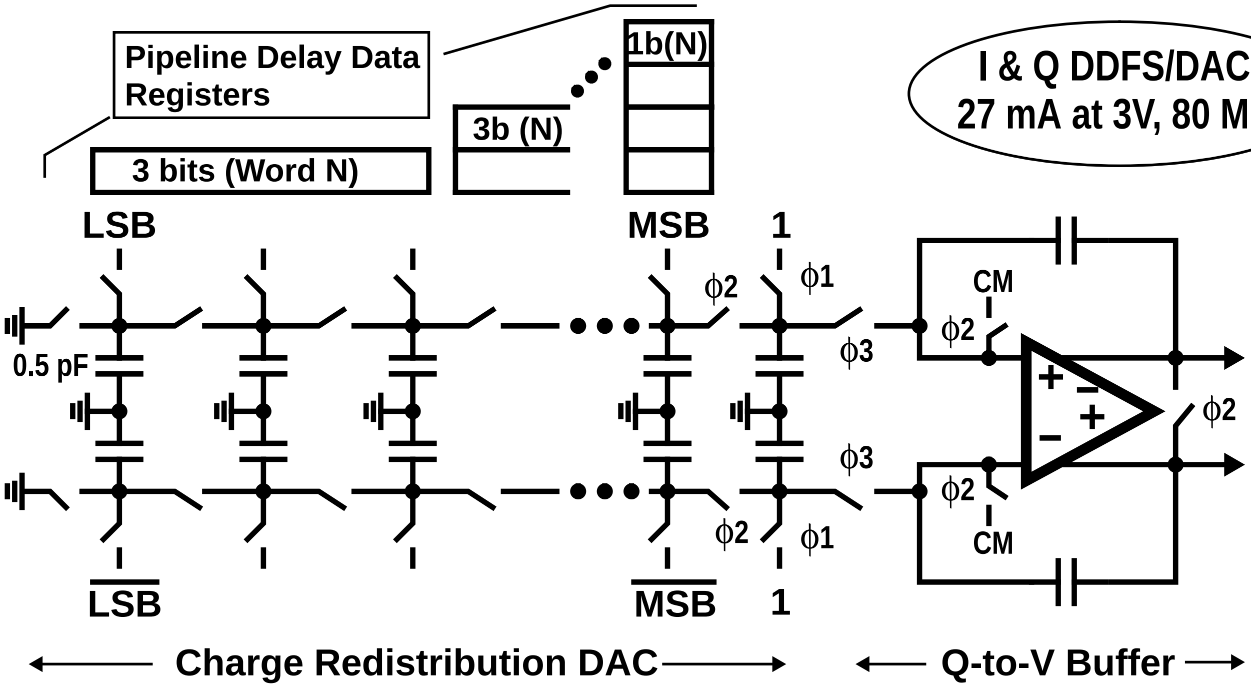
- Amplifier attains 42% power conversion efficiency at +15 dBm output power
- Binary-weighted array of FETs gives 36 dB of power control (6-b word)
- Inductively-loaded preamp drives FETs above 3-V supply
- Off-chip matching network filters out harmonics

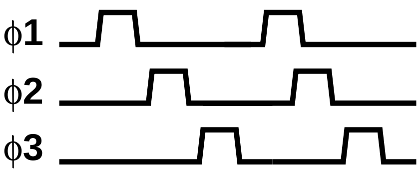
Frequency-Hopped Synthesizer



- DDFS produces samples of a sinewave at a frequency selected by 11-b word; instantly agile frequency source
- DDFS output range is 0→13 MHz; *adding* up-converted outputs produces SSB 915→928 MHz; *subtracting* them produces 902→915 MHz
- 8-b matching required between channels for adequate image suppression

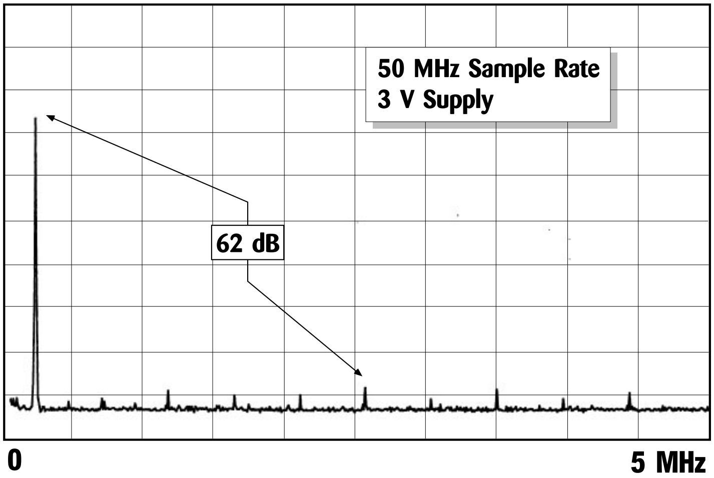
10-b, 80 MHz D-A Converter

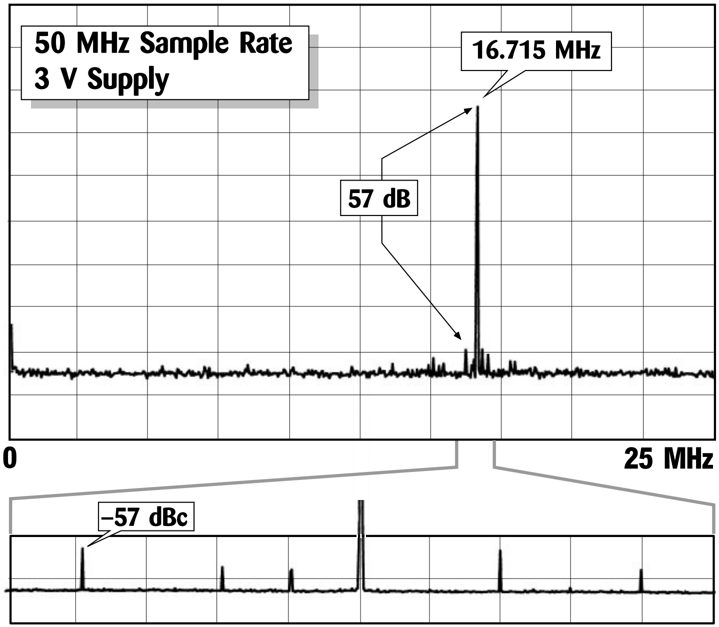




- Low-power through differential implementation using quasi-passive charge-redistribution pipelines
- Linearity limited by capacitance mismatch, voltage-dependent parasitics
- Glitch free!

Measured DDFS/DAC Spectral Outputs

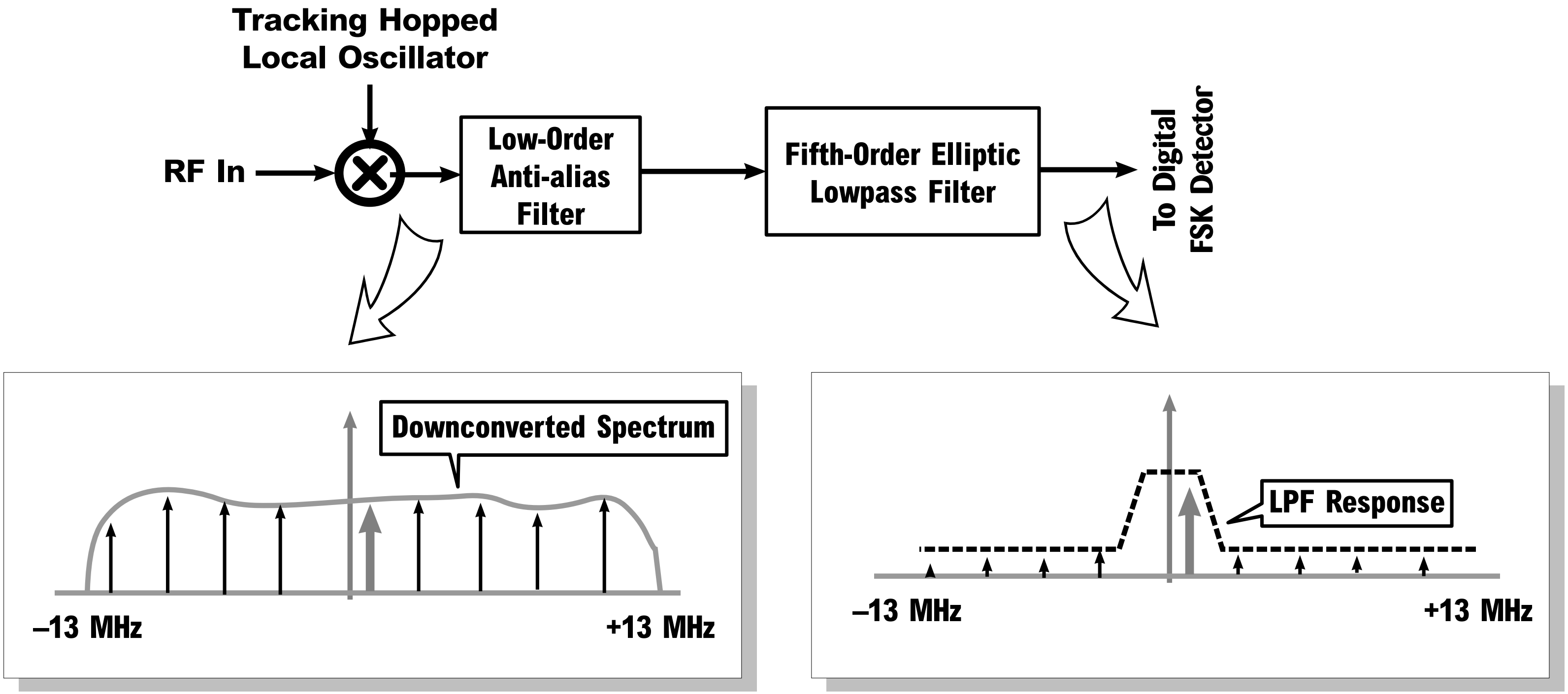




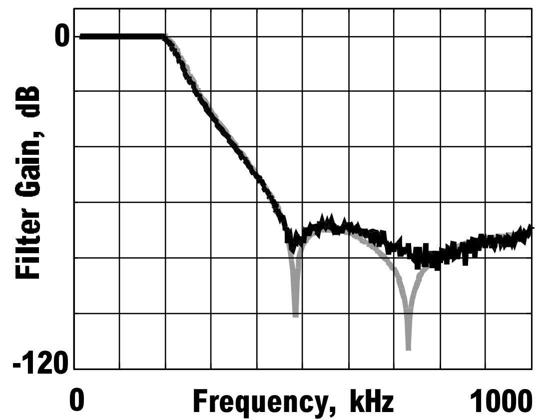
- **Spurious level as predicted**
  - set by capacitor mismatch

- **Inter-cell capacitance causes non-linearity at high frequency**

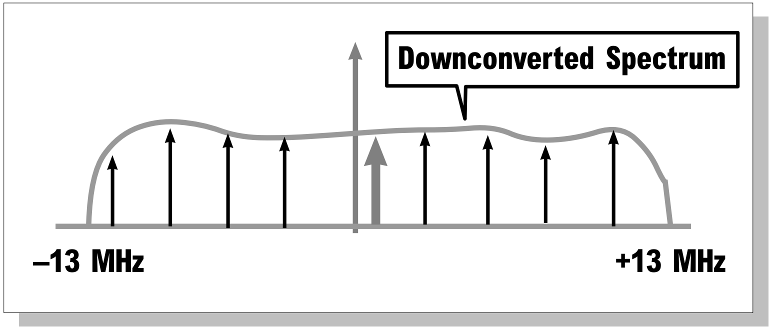
Baseband Tone-Select Filter

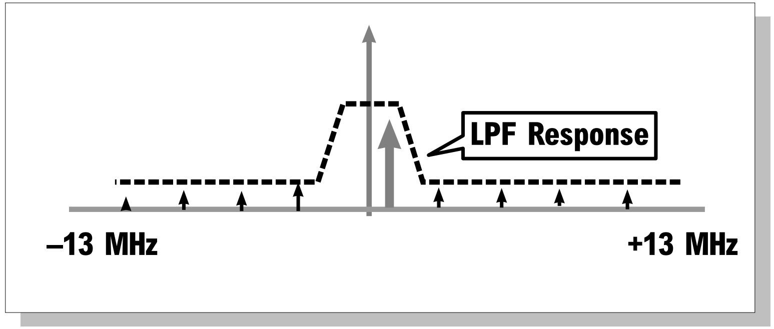


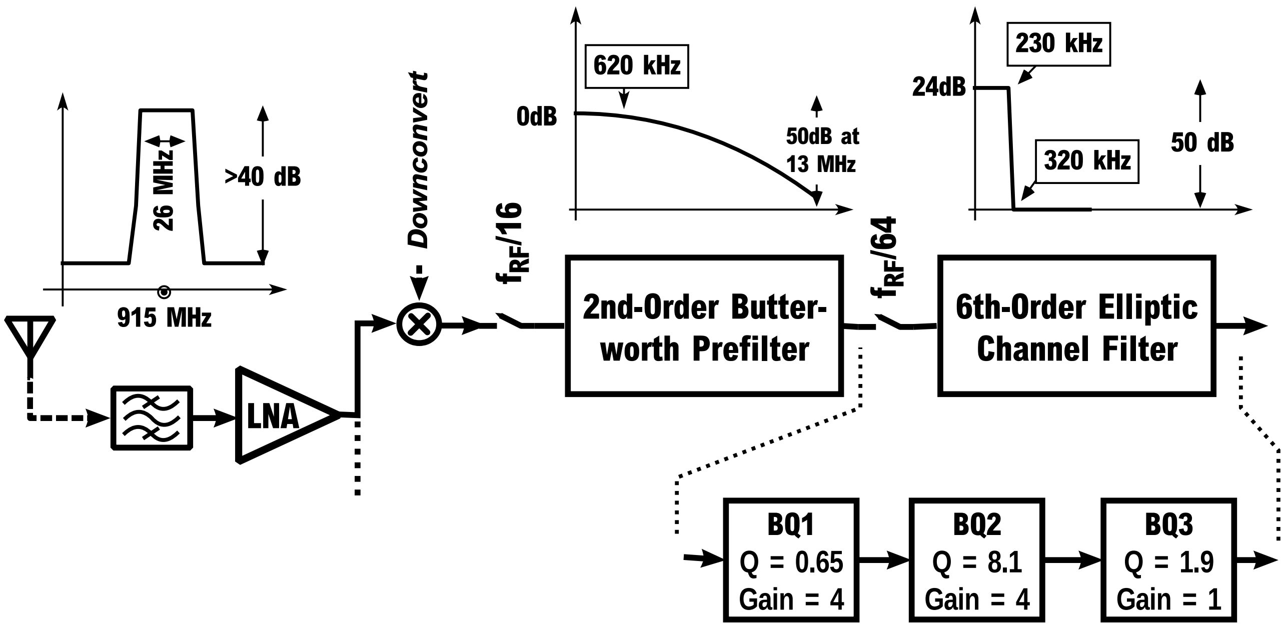
- 5th-order Elliptic LPF with 200-kHz cutoff implemented as SCF; dissipates 15 mW from 3-V at 5 MHz sample rate. Operates up to 20 MHz. 60 dB stopband attenuation.
- LPF sets *noise bandwidth* of entire system



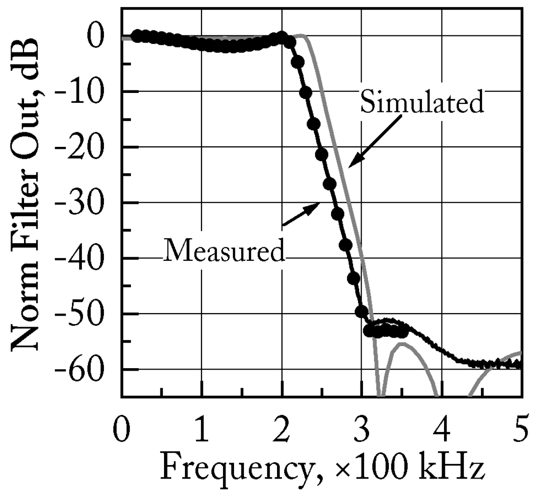
Lowpass Channel-Select Filter

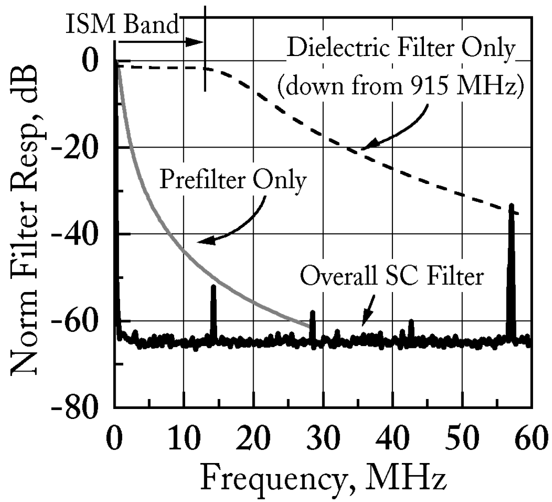


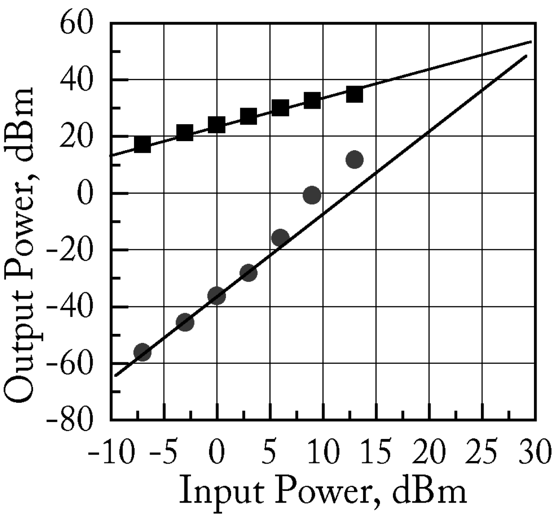


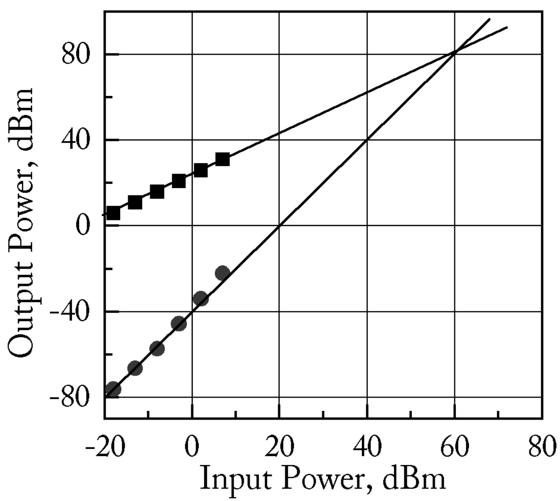


Measured Filter Performance



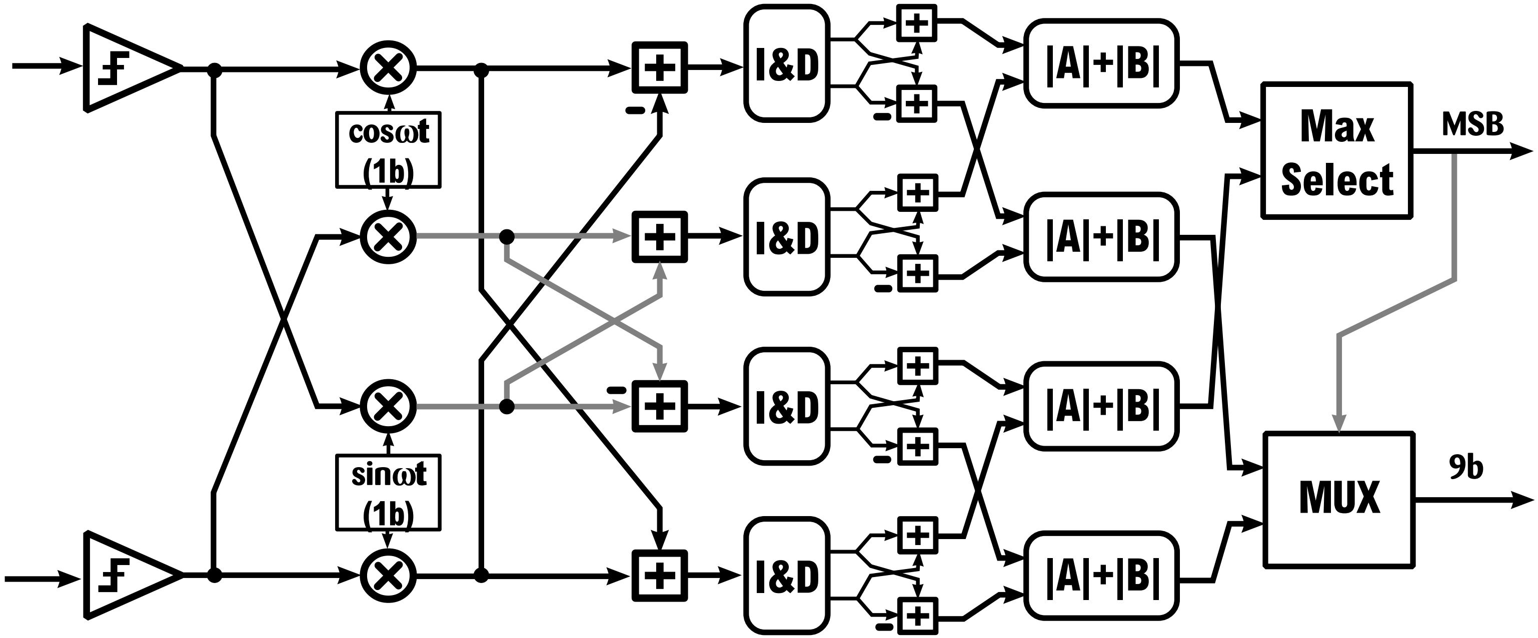






- 70 nV/Hz in passband
- 4.6 mA from 3V
- 200 pF total on-chip capacitance

Digital Tone Detector



- 1-bit oversampled correlator (programmable oversample rate)
- Multipliers are switches, integrators are accumulators
- 1.9 sq mm active area implementation will dissipate 2 mW

Rationale Underlying UCLA Low-Power Transceiver

- Radio paging receiver is the most evolved low-energy wireless device today. Receives 500 to 1000 b/s at 400 MHz to 900 MHz.
- Long battery life obtained through very high level of integration (two chips) and optimized system design
- UCLA transceiver uses this as a model. Key extensions are:
  - ✓ *Two-way communication*
  - ✓ *Much higher data rate ⇨160 kb/s (programmable)*
  - ✓ *Robust operation in multipath environment ⇨ Diversity*
  - ✓ *Large multi-user capacity ⇨ CDMA spread-spectrum*

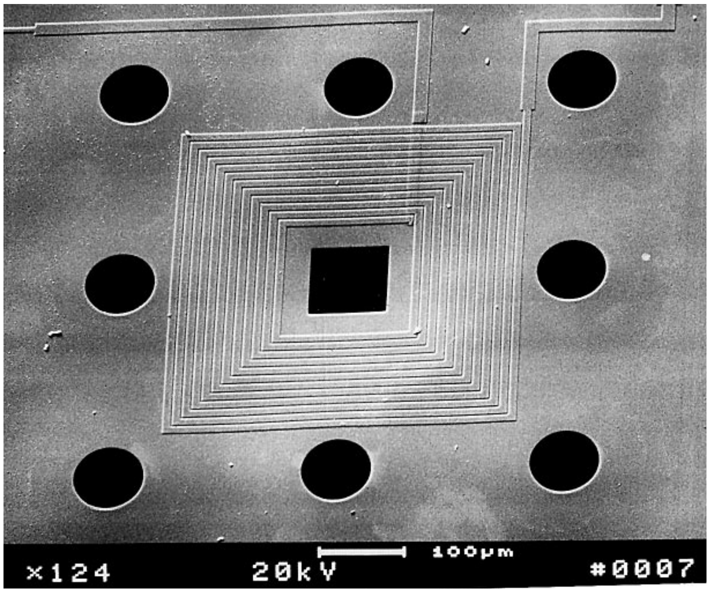
Features
- ♦ Binary FSK modulation of carrier (like pager)
- ♦ Frequency-hopped spread-spectrum
- ♦ Simple demodulation after de-hopping (like pager)
- ♦ Two-chip transceiver (like paging receiver)

New Technology for Etching Inductors

Need fast etchant in p+ doped substrates

Should minimally etch exposed metallization

Xenon DiFluoride (XeF_2) gas-phase etchant



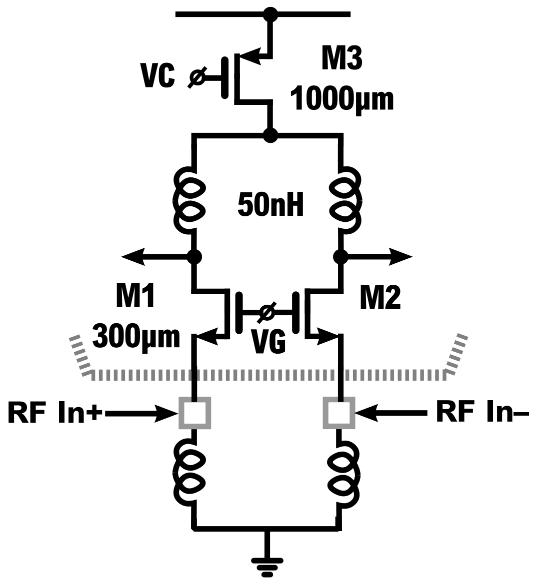
- Etches hemispherical pits anisotropically through array of small holes in oxide
- Depth of etching may be visually monitored through semi-transparent nitride

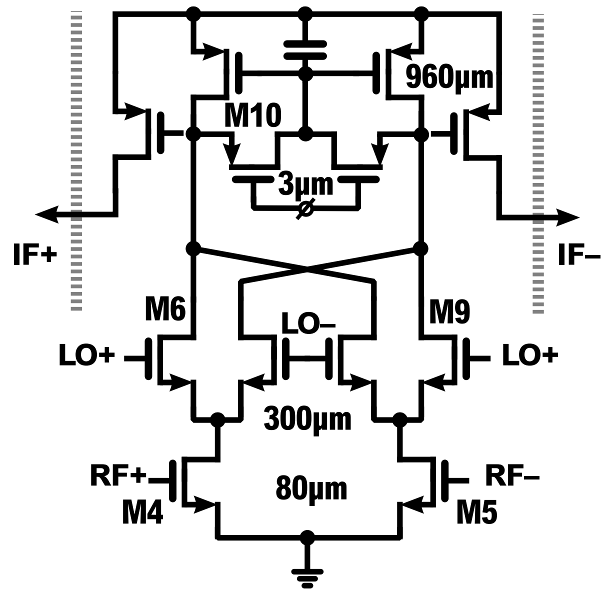
1 GHz Continuous-Time LNA and Mixer

A demonstration of the fundamental capability of MOSFETs to attain *low noise* and *wide dynamic range*, at *low power*

1-μm CMOS operating at 3V; matched to 50Ω at input

Drain 8 mA from 3V

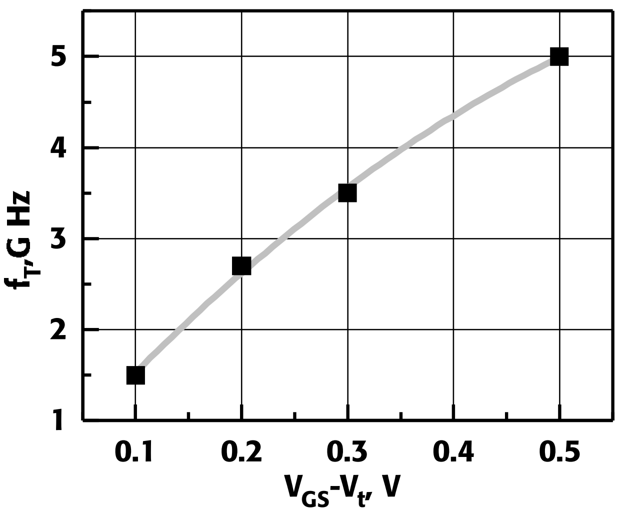




LNA Design Rationale

$$\text{Gain} = Q^2 R_s \times g_m = \frac{1}{(\omega_0 C)^2 R_s \times 50\Omega} \approx \left(\frac{50\Omega}{R_s}\right)\left(\frac{\omega_T}{\omega_0}\right)^2$$

Measured f_T vs V_{GS}–V_t



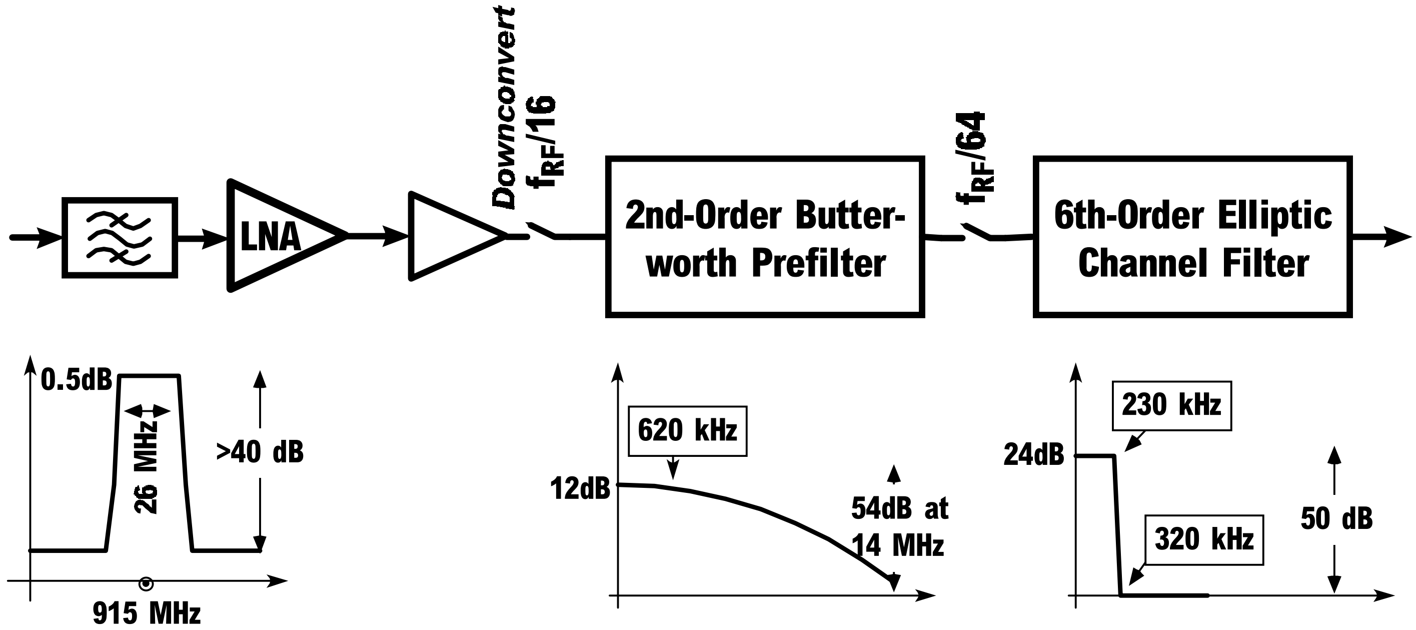
50 nH on-chip inductor load

Rs ≃ 50Ω

23 dB gain requires bias at $(V_{GS}-V_t)=0.6V$ for sufficiently high f_T

LNA + mixer drain 8 mA from 3 V

Channel-Select Filter



Current drain of active filter ~ 3.5 mA

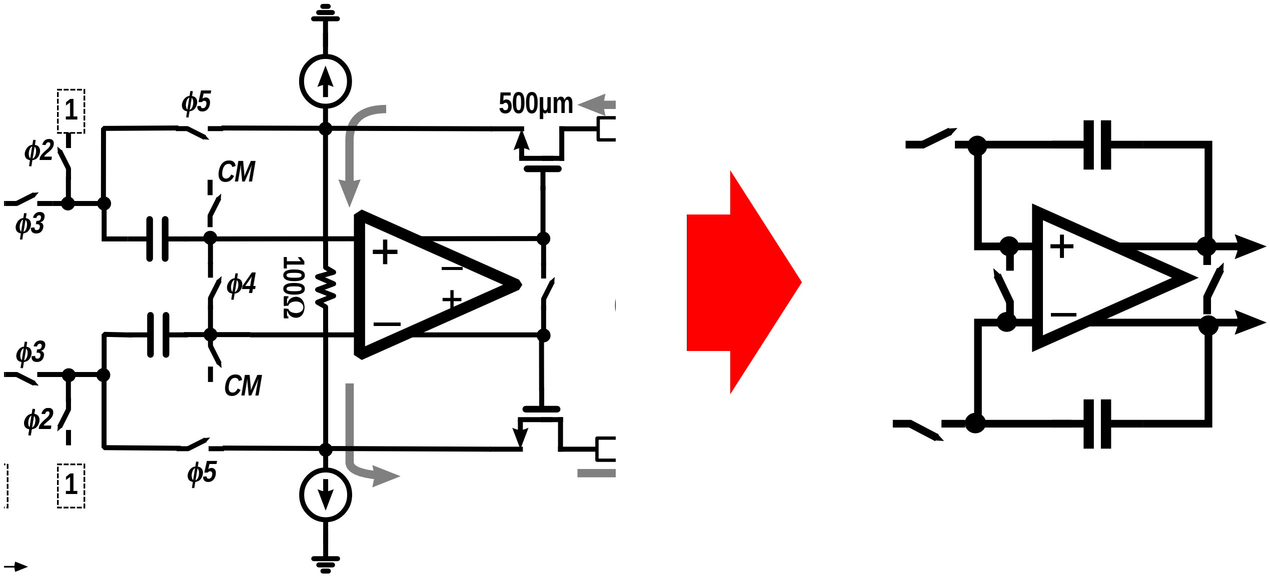
Input-referred noise ~ 40 nV/$\sqrt{\text{Hz}}$

Capacitor spread = 108

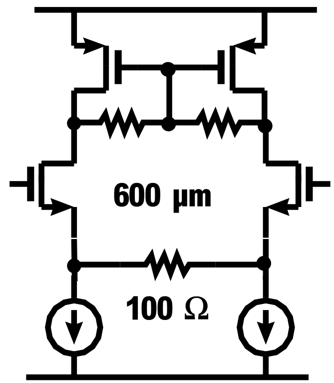
Input capacitor ~ 0.45 pF

Output compression point ~ 2 V ptp

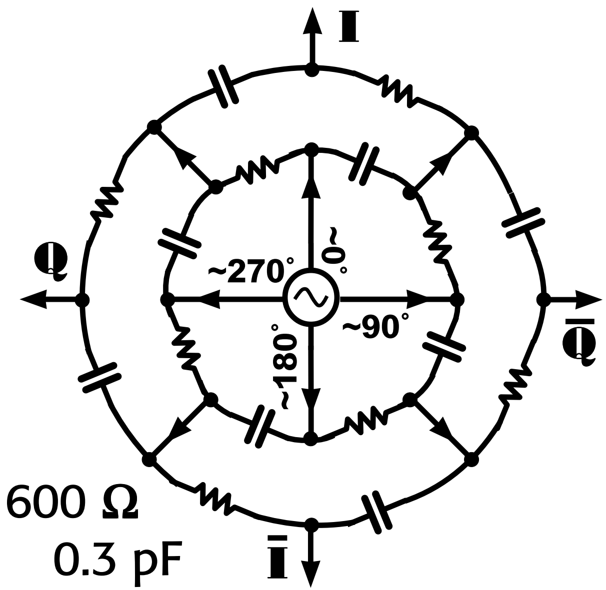
Increasing DDFS/DAC Clock Frequency



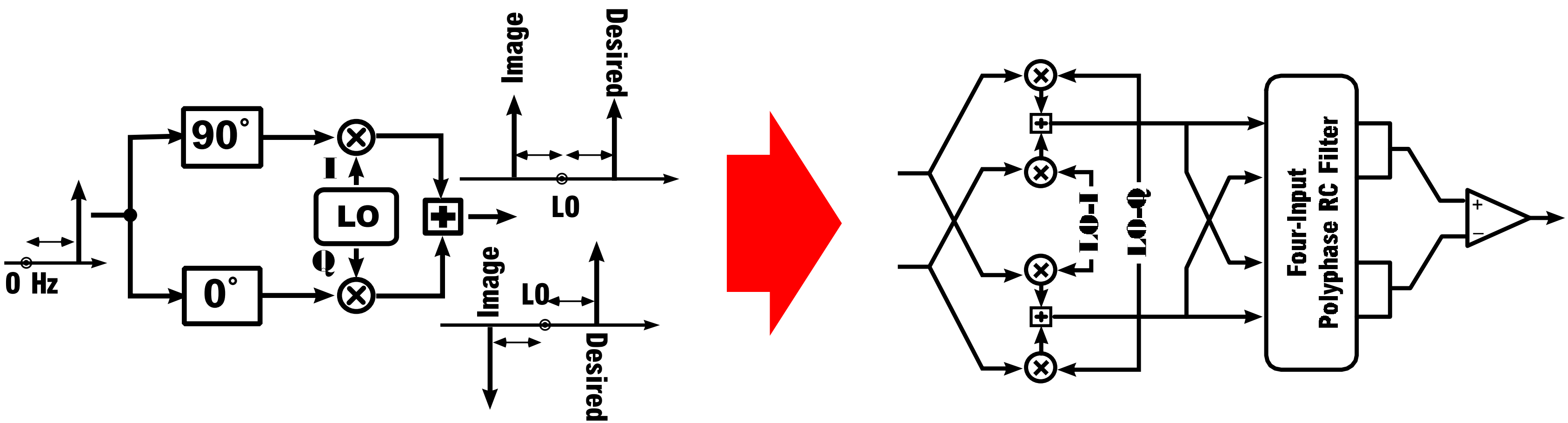
- Eliminate two clock phases, φ4 and φ5, in buffer driving on-chip capacitive load
- Rescale DDFS. Carry-select adder in accumulator.
- Use open-loop buffer to drive polyphase filter through four-FET switch upconversion mixers
- 3rd-order distortion, including buffer < −45 dB



Polyphase Filter for Sideband Selection



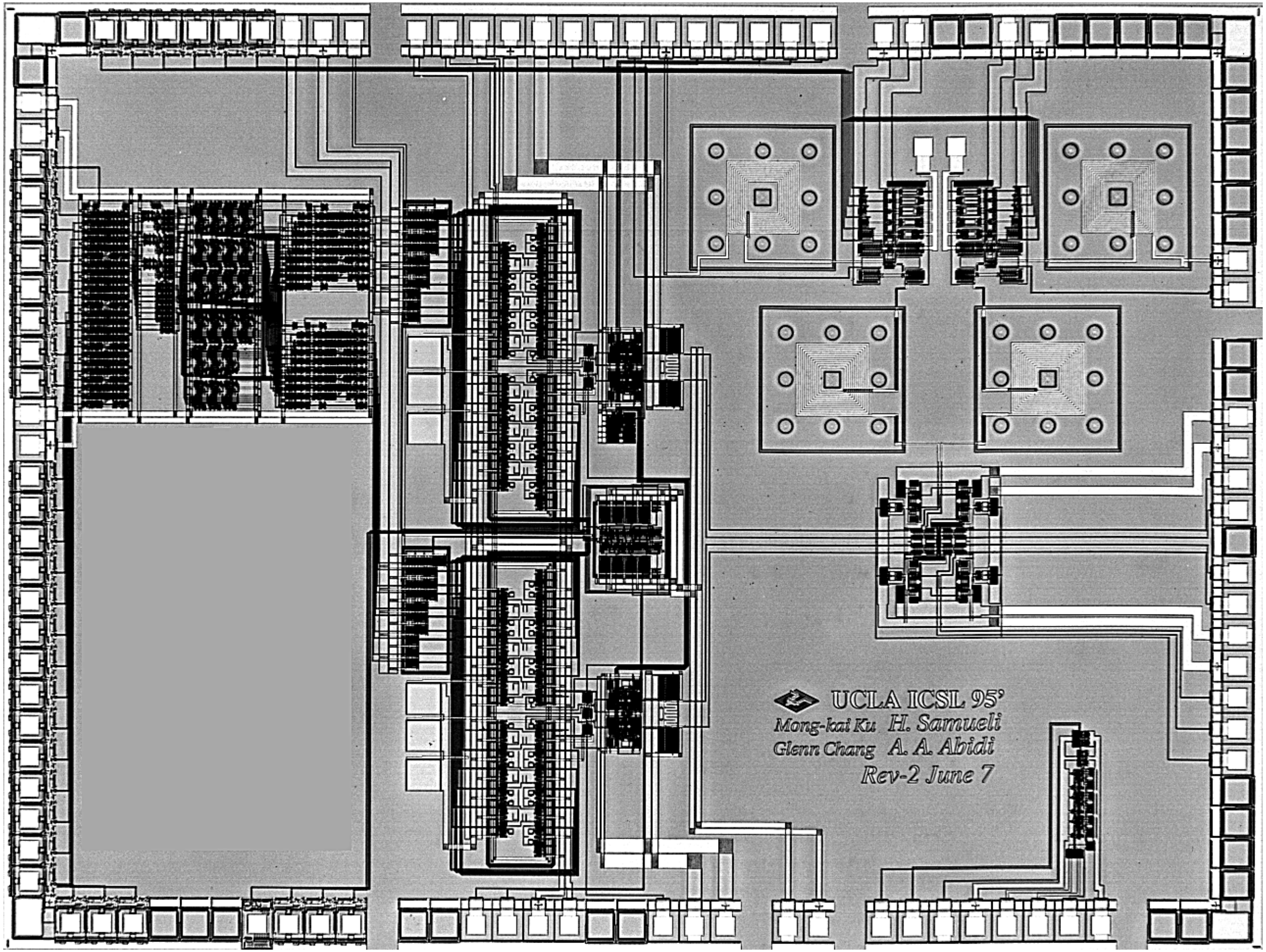
- Extension of the RC-CR phase-shift network, with four-phase inputs and outputs
- Reinforces one sequence of quadrature phases (clockwise, say), while attenuating the other
- Robust against component mismatches (order-of-magnitude better than single-phase network)
- Similarly selects one sideband after upconversion (60 dB rejection with 10° phase error in LO)



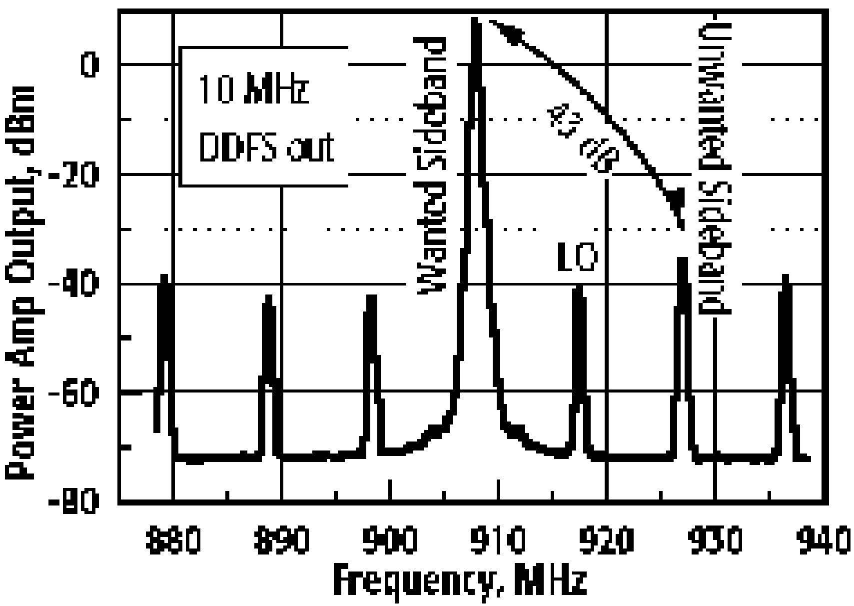
Transmitter Test Chip

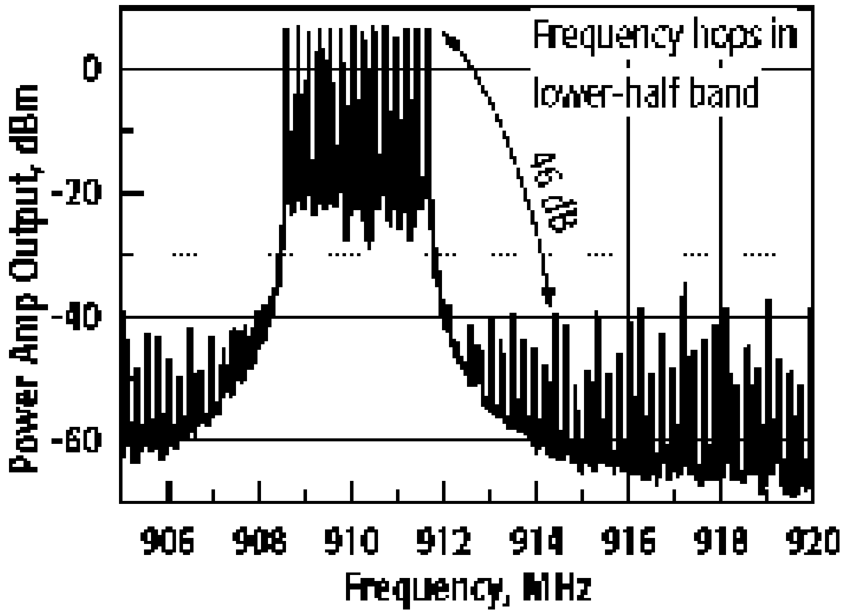
6×3.8 mm active area

65 mA active current



Transmitter Output Spectra

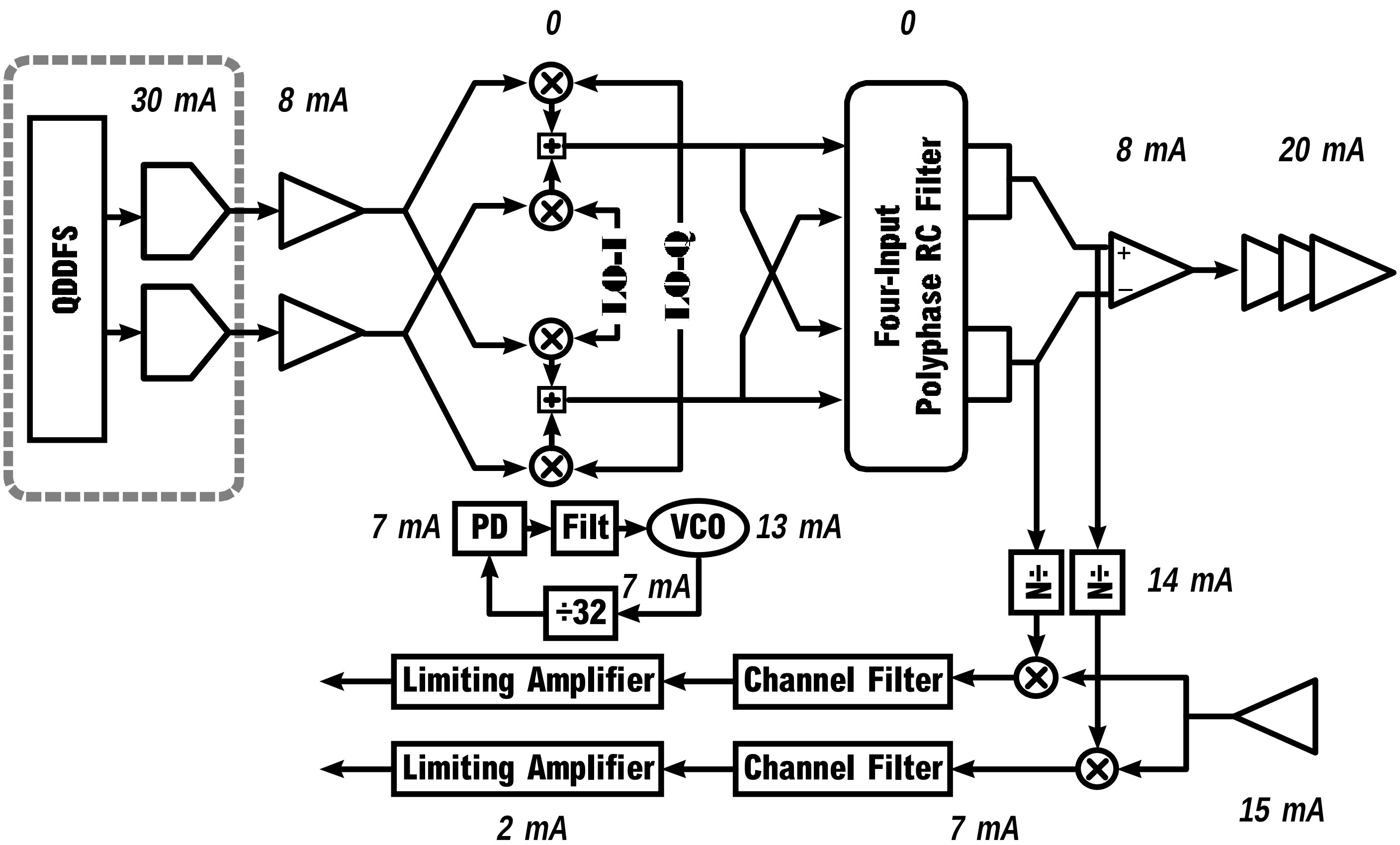




No off-chip filter at power amplifier output

Measurements at mid-range level +5 dBm

Current Drain in Transceiver Parts



Measured Performance of Front-End