National Semiconductor

ADVANCE INFORMATION
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LMX3160 Single Chip Radio Transceiver

General Description

The Single Chip Radio Transceiver is a monolithic, integrated radio transceiver optimized for use in the Digital European Cordless Telecommunications (DECT) system as well as other mobile telephony and wireless communications applications. It is fabricated using National's ABiC V BiCMOS process (f_T = 18 GHz).

The Single Chip Radio Transceiver contains both transmit and receive functions. The transmitter includes a 1.1 GHz phase locked loop (PLL), a frequency doubler, and a high frequency buffer. The receiver consists of a 2.0 GHz low noise mixer, an intermediate frequency (IF) amplifier, a high gain limiting amplifier, a frequency discriminator, a received signal strength indicator (RSSI), and an analog DC compensation loop. The PLL, doubler, and buffers can be used to implement open loop modulation. The circuit features an onboard voltage regulator to allow wide supply voltages. In addition, the on board voltage regulator has two outputs for regulated discrete stages in the Rx and Tx chain.

The IF amplifier, high gain limiting amplifier, and discriminator operate in the 40 to 150 MHz frequency range, and the total IF gain is 85 dB. The use of the limiter and the discriminator provides a low cost, high performance demodulator for communications systems. The RSSI output can be used for channel quality monitoring.

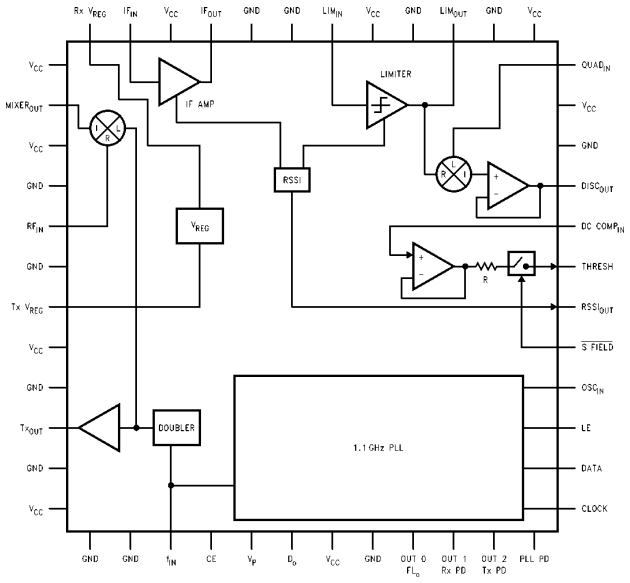
The Single Chip Radio Transceiver is available in a 48-pin 7mm X 7mm X 1.4mm PQFP surface mount plastic package.

Features

- Single chip solution for DECT RF transceiver
- RF sensitivity to −93 dBm; RSSI sensitivity to −100 dBm
- Two regulated voltage outputs for discrete amplifier V_{CC}
- High gain (85 dB) intermediate frequency strip
- Allows unregulated 3.0V–5.5V supply voltage range
- Power down mode for increased current savings
- System noise figure 5.4 dB (typ)

Applications

- Digital European Cordless Telecommunications (DECT)
- Portable wireless communications (PCS/PCN, cordless)
- Wireless local area networks (WLANs)
- Other wireless communications systems



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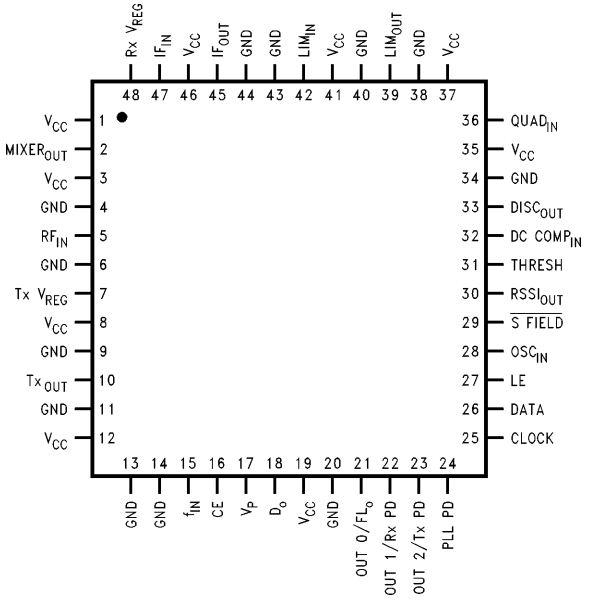
This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.

RRD-B30M115/Printed in U. S. A.

LMX3160 Pin Diagram



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Pin No.	Pin Name	I/O	Description
1	V_{CC}	—	Power supply voltage input to mixer. Connect to VBAT
2	$MIXER_{OUT}$	O	IF output signal of the mixer.
3	V_{CC}	—	Power supply voltage input to mixer. Connect to VBAT
4	GND	—	Ground.
5	RF_{IN}	I	RF input to the mixer.
6	GND	—	Ground.
7	Tx V_{REG}	O	Supply voltage to external gain stage.
8	V_{CC}	—	Power supply voltage input to analog sections of doubler/PLL. Connect to VBAT
9	GND	—	Ground.
10	Tx_{OUT}	O	Doubler output.
11	GND	—	Ground.
12	V_{CC}	—	Power supply voltage input to analog sections of doubler/PLL. Connect to VBAT
13	GND	—	Ground.
14	GND	—	Ground.
15	f_{IN}	I	RF Input to doubler and PLL.
16	CE	I	Chip Enable. LOW powers down entire part. Before taking HIGH all μwire instructions should be loaded for R, N, F latches. Taking CE HIGH will power up the appropriate chip blocks depending on the state of bits F6, F7, F14, and F15. The CE state change will also load the PLL N and R counters to the correct divide ratios.

LMX3160 Pin Diagram (Continued)

Pin No.	Pin Name	I/O	Description
17	V_P	—	Power supply for charge pump.
18	D_o	O	Internal charge pump output. For connection to a loop filter for driving the input of an external VCO.
19	V_{CC}	—	Power supply input for CMOS section of PLL. Connect to VBAT
20	GND		Ground.
21	Out 0/FL_o	I/O	Programmable CMOS output. Can be used for FastLock™ output (See Programmable Modes).
22	Out 1/Rx PD	I/O	Programmable CMOS output. Can be used for hardwire receiver power down (See Programmable Modes).
23	Out 2/Tx PD	I/O	Programmable CMOS output. Can be used for hardwire transmitter power down (See Programmable Modes).
24	PLL PD	I	PLL PD = LOW for PLL normal operations. PLL PD = HIGH for PLL power saving.
25	Clock	I	High impedance CMOS clock input.
26	Data	I	Binary serial data input. Data entered MSB first. High impedance CMOS input.
27	LE	I	Load enable input.
28	OSC_{IN}	I	Oscillator input.
29	$\overline{\text{S Field}}$	I	DC compensation circuit enable. While LOW, the DC compensation circuit is enabled, and the threshold is updated through the DC compensation loop. While HIGH, the switch is opened, and the comparator is held by the external capacitor.
30	$RSSI_{OUT}$	O	Voltage output of the received signal strength indicator (RSSI).
31	Thresh	O	Threshold level to external comparator.
32	DC $COMP_{IN}$	I	Input to DC compensation circuit.
33	$DISC_{OUT}$	O	Demodulated output of discriminator.
34	GND	—	Ground.
35	V_{CC}	—	Power supply input to discriminator circuit. Connect to VBAT
36	$QUAD_{IN}$	I	Quadrature input.
37	V_{CC}	—	Power supply input to limiter output stage. Connect to VBAT
38	GND	—	Ground.
39	LIM_{OUT}	O	Limiter output to the quadrature tank.
40	GND	—	Ground.
41	V_{CC}	—	Power supply input for limiter. Connect to VBAT
42	LIM_{IN}	I	IF input to the limiter.
43	GND	—	Ground.
44	GND	—	Ground.
45	IF_{OUT}	O	IF output to bandpass filter.
46	V_{CC}	—	Power supply input for IF amplifier. Connect to VBAT
47	IF_{IN}	I	IF input to IF amplifier.
48	Rx V_{REG}	—	Supply voltage to external LNA.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Supply Voltage (V_{CC})	−0.3V to +6.5V
V_P	−0.3V to +6.5V
Voltage on Any Pin with GND = 0V (V_I)	−0.3V to +6.5V
Storage Temperature Range (T_S)	−65°C to +150°C
Lead Temp. (solder, 4 sec)(T_L)	+260°C

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Recommended Operating Conditions

Supply Voltage (V_{CC})	3.0V to 5.5V
Operating Temperature (T_A)	−10°C to +70°C

Electrical Characteristics

The following specifications are guaranteed over the recommended operating conditions unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Rx I_{CC}	Receive Mode Current Consumption (Note 1)	Tx PLL Powered Down		38	45	mA
Tx I_{CC}	Transmit Mode Current Consumption (Note 2)	Rx PLL Powered Down		20	25	mA
I_{PD}	Power Down Current	Tx, Rx, PLL Off		1	10	μA
f_{RF}	RF Frequency Range		1.7		2.0	GHz
f_{max}	Maximum IF Input Frequency		120	150		MHz
f_{min}	Minimum IF Input Frequency			18	20	MHz
MIXER		f_{IN} = 1.9 GHz				
NF	Single Side Band Noise Figure			5.9	7	dB
GA	Gain		16	18		dB
OIP3	Output Intercept Point		−2	1		dBm
RF−RL	RF Return Loss	Z_o = 50Ω		15		dB
IF−RL	IF Return Loss	Z_o = 200Ω		15		dB
f_{IN}−RF	f_{IN} to RF Isolation			30		dB
f_{IN}−IF	f_{IN} to IF Isolation			30		dB
RF−IF	RF to IF Isolation			30		dB

Electrical Characteristics The following specifications are guaranteed over the recommended operating conditions unless otherwise specified (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
IF AMPLIFIER		f_{IN} = 120 MHz				
NF	Noise Figure			6	8	dB
Av	Gain		20	25		dB
OIP3	Output Intercept Point		6	7		dBm
Z_{IN}	Input Impedance			200		Ω
Z_{OUT}	Output Impedance			200		Ω
IF LIMITER		f_{IN} = 120 MHz				
NF	IF Limiter Noise Figure			10	12	dB
Av	Limiter Gain		55	60		dB
Sens	Limiter/Disc. Sensitivity	BER = 10^{-3}		−65		dBm
IF_{IN}	IF Limiter Input Impedance			200		Ω
IF_{OUT}	IF Limiter Output Impedance			1000		Ω
V_{max}	Maximum Input Voltage Level		500			mV_{PP}
V_{OUT}	Output Swing			500		mV_{PP}
	Dynamic Range			60		dB
DISCRIMINATOR		f_{IN} = 120 MHz				
V_{OUT}	Discriminator Output Peak to Peak Voltage		250	400		mV
V_{OS}	Disc. Output DC Voltage		1.4		1.7	V
$DISC_{OUT}$	Disc. Output Impedance			150		Ω
RSSI		f_{IN} = 120 MHz				
RSSI	RSSI Dynamic Range		70	80		dB
$RSSI_{OUT}$	RSSI Output Voltage	Pin = −85 dBm	0.1	0.25	0.4	V
		Pin = 0 dBm	1.15	1.5	1.8	V
	RSSI Slope	Pin = −75 to −25 dBm	11	20		mV/dB
	RSSI Linearity			3		dB
FREQUENCY DOUBLER		f_{OUT} = 1.89 GHz				
f_{IN}	Input Frequency Range		885		950	MHz
V_{IN}	Input Signal Level	Z_{IN} = 200Ω	−14	−11.5	−9	dBm
Z_o	Output Impedance		45	60	80	Ω
	Fundamental Rejection (Note 3)	V_{IN} = 450 mV_{PP}		30		dB
	Harmonic Suppression (Note 3)	V_{IN} = 450 mV_{PP}		20		dB
P_{OUT}	Output Power		−10	−8		dBm

Electrical Characteristics The following specifications are guaranteed over the recommended operating conditions unless otherwise specified (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
FREQUENCY SYNTHESIZER						
V_{OSC}	Oscillator Sensitivity		0.5	1.0		V_{PP}
$I_{Do\text{-}source}$	Charge Pump Output Current	$V_{do} = V_P/2$, I_{cpo} = LOW (Note 4)		−1.5		mA
$I_{Do\text{-}sink}$		$V_{do} = V_P/2$, I_{cpo} = LOW (Note 4)		1.5		mA
$I_{Do\text{-}source}$		$V_{do} = V_P/2$, I_{cpo} = HIGH (Note 4)		−6.0		mA
$I_{Do\text{-}sink}$		$V_{do} = V_P/2$, I_{cpo} = HIGH (Note 4)		6.0		mA
$I_{Do\text{-}Tri}$		$0.5 \le V_{do} \le V_P - 0.5$ $T_A = 25°C$	−1.0	0.1	1.0	nA
V_{OH}	High-Level Output Voltage	$I_{OH} = -1.0$ mA	V_{CC} −0.4			V
V_{OL}	Low-Level Output Voltage	$I_{OL} = 1.0$ mA			0.4	V
V_{IH}	High-Level Input Voltage		V_{CC} −0.8			V
V_{IL}	Low-Level Input Voltage				0.8	V
I_{IN}	Input Current	$GND < V_{IN} < V_{CC}$	−1.0		1.0	mA
t_{CS}	Data to Clock Set Up Time	See Data Input Timing	50			ns
t_{CH}	Data to Clock Hold Time	See Data Input Timing	10			ns
t_{CWH}	Clock Pulse Width High	See Data Input Timing	50			ns
t_{CWL}	Clock Pulse Width Low	See Data Input Timing	50			ns
t_{ES}	Clock to Load Enable Set Up Time	See Data Input Timing	50			ns
t_{EW}	Load Enable Pulse Width	See Data Input Timing	50			ns
DC COMPENSATION SAMPLE AND HOLD CIRCUIT						
V_{OS}	Input Offset Voltage				3	mV
$V_{I/O}$	Input/Output Voltage Swing	Centered at 1.5V		1.0		V_{PP}
R_{SH}	Sample and Hold Resistor		224		336	Ω
D_V	Threshold Input Voltage Droop	$C_{hold} = 2700$ pF		1	10	mV/ms

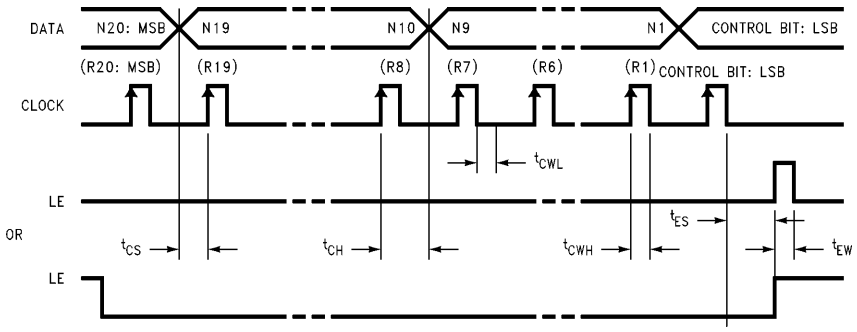
Note 1: This includes 5 mA current sourced from the Rx V_{REG} pin for the external receive LNA as shown in the application diagram.

Note 2: This includes 5 mA current sourced from the Tx V_{REG} pin for the external transmit buffer used before the power amplifier as shown in the application diagram.

Note 3: Measured at the output of external gain stage.

Note 4: See programmable modes for I_{cpo} description.

Serial Data Input Timing



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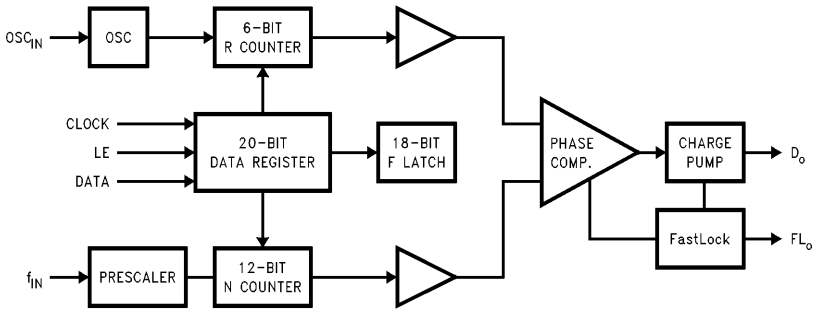
Notes: Parenthesis data indicates programmable reference divider data.
Data shifted into register on clock rising edge.
Data is shifted in MSB first.

Test Conditions: The Serial Data Input Timing is tested using a symmetrical waveform around $V_{CC}/2$. The test waveform has an edge rate of 0.6V/ns with amplitudes of 2.2V @ V_{CC} = 3.0V and 2.6V @ V_{CC} = 5.5V.

PLL Functional Description

The simplified block diagram below shows the 20-bit data register, 18-bit F latch, 12 bit N counter, and 6 bit R counter.



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PLL Functional Description (Continued)

The data stream is clocked on the rising edge of LE into the DATA input, MSB first. The last two bits are the control bits. DATA is transferred into the counters as follows:

Control Bits		DATA Location
C1	C2	
0	0	N Counter
0	1	R Counter
1	X	F Latch

X = Dont Care

Programmable Divider (N Counters)

The N counter consists of the 6-bit swallow counter (A counter) and the 6-bit programmable counter (B counter). When the control bits are ''00'' data is transferred from the 20-bit shift register into two 6-bit latches. One latch sets the A counter while the other sets the B counter, MSB first. Serial data format is shown below.

LSB **MSB**

C1	C2	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11	N12	X	X	X	X	X	X
Control Bits		Divide Ratio of Programmable Divider, N												Don't Care					

6-Bit Swallow Counter Divide Ratio (A Counter)

Divide Ratio A	N6	N5	N4	N3	N2	N1
0	0	0	0	0	0	0
1	0	0	0	0	0	1
*	*	*	*	*	*	*
63	1	1	1	1	1	1

Notes: Divide ratio: 0 to 63

B ≥ A

6-Bit Programmable Counter Divide Ratio (B Counter)

Divide Ratio B	N12	N11	N10	N9	N8	N7
3	0	0	0	0	1	1
4	0	0	0	1	0	0
*	*	*	*	*	*	*
63	1	1	1	1	1	1

Notes: Divide ratio: 3 to 63

B ≥ A

Programmable Reference Dividers (R Counters)

If the control bits are ''01'' data is transferred from the 20-bit shift register into a latch which sets the 6-bit R counter. Serial data format is shown below.

LSB **MSB**

C1	C2	R1	R2	R3	R4	R5	R6	X	X	X	X	X	X	X	X	X	X	X	X

Control Bits — Divide Ratio of Reference Divider — Don't Care

Divide Ratio R	R6	R5	R4	R3	R2	R1
3	0	0	0	0	1	1
4	0	0	0	1	0	0
*	*	*	*	*	*	*
63	1	1	1	1	1	1

Note: Divide ratio: 3 to 63

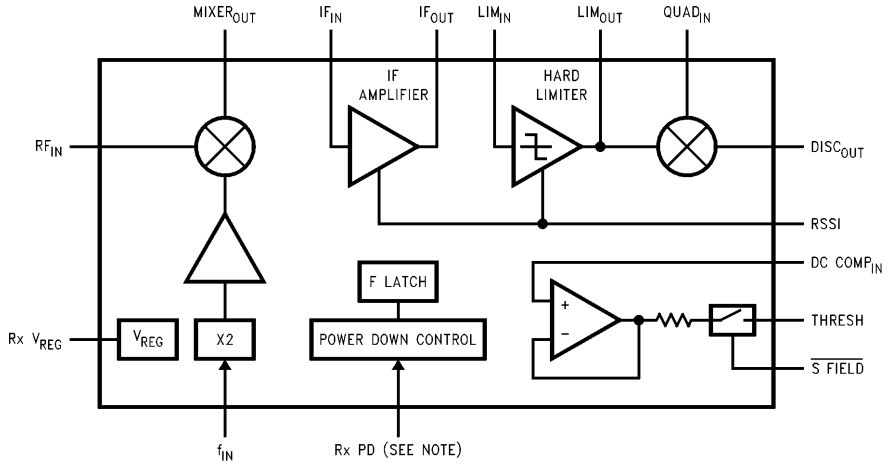
Pulse Swallow Function

$f_{VCO} = [(P \times B) + A] \times f_{OSC}/R$

- f_{VCO}: Output frequency of external voltage controlled oscillator (VCO)
- B: Preset divide ratio of binary 6-bit programmable counter (3 to 63)
- A: Preset divide ratio of binary 6-bit swallow counter ($0 \leq A \leq P$, $A \leq B$)
- f_{OSC}: Output frequency of the external reference frequency oscillator
- R: Preset divide ratio of binary 6-bit programmable reference counter (3 to 63)
- P: Preset modulus of dual modulus prescaler (32 or 64)

Receiver Functional Description

The simplified block diagram below shows the mixer, IF amplifier, limiter, and discriminator. In addition, the DC compensation circuit, doubler, and voltage regulator (for external LNA) are shown.



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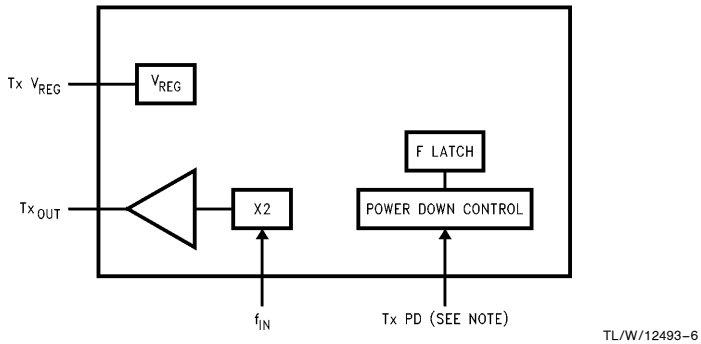
Note: Receiver power down can be controlled by software through the F Latch or hardwire through the Rx PD pin. This is determined by the state of F14 and F15 (See Programmable Modes).

Transmitter Functional Description

The simplified block diagram below shows the doubler and voltage regulator (for external transmit gain stage).



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Note: Transmitter power down can be controlled by software through the F Latch or hardwire through the Rx PD pin. This is determined by the state of F14 and F15 (See Programmable Modes).

Programmable Function Latch (F Latch)

If the control bits are ''1X'' data is transferred from the 20-bit shift register into the 18-bit F latch. Serial data format is shown below.

LSB																			**MSB**
C1	C2	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15	F16	F17	F18
Control Bits																			

Programmable Modes

Several modes of operation can be programmed with the function register bits F1−F18, including the phase detector polarity, charge pump TRI-STATE® and CMOS outputs. In addition, software or hardwire power down modes may be selected with bits F14 and F15. The programmable modes are latched in when the control bits are: C1 = 1, C2 = X. Truth tables for the programmable modes are shown in Tables I−III.

TABLE I. Programmable Modes

F1	Prescaler Mod Select (32/64)
F2	Phase Detector Polarity
F3	Charge Pump Current
F4	Charge Pump TRI-STATE
F5	Don't Care
F6	Receive Section Power Down
F7	Transmit Section Power Down
F8	Out 0 CMOS Output/FastLock Output
F9	Out 1 CMOS Output/Receive Section Power Down Input
F10	Out 2 CMOS Output/Transmit Section Power Down Input
F11	Don't Care
F12	FastLock Auto/man select
F13	Out 0 Normal CMOS/FastLock Switch
F14	Mode Select. See Mode Select Table
F15	Mode Select. See Mode Select Table
F16	Auto FastLock Counter Bit #16
F17	Auto FastLock Counter Bit #32
F18	Auto FastLock Counter Bit #64

Functional Description

F1	Pre-scaler modules select. LOW selects 32/33 and HIGH selects 64/65.
F2	Phase Detector Polarity. F2 is used to reverse the polarity of the phase detector. Depending upon V_{CO} characteristics, F2 should be set accordingly: When VCO characteristics are positive, F2 should be set HIGH; When VCO characteristics are negative, F2 should be set LOW.
F3	Charge pump current. LOW selects low charge pump current (1X I_{cpo}). High selects HIGH charge pump current (4X I_{cpo}).
F4	Charge Pump TRI-STATE.
F5	Don't Care.
F6−F7	Power down. When F14 = 0 and F15 = 0, F6 controls the state of the receive section and F7 controls the state of the transmit section. A LOW powers up the section while a HIGH powers down the section.
F8−F10	CMOS Outputs. When F13 is LOW, F8 controls sets state of Out 0 (pin 21). When in normal power down mode (F14 = 0, F15 = 0), F9 and F10 sets the state of Out 1 (pin 22) and Out 2 (pin 23) respectively.
F11	Don't Care.
F12	FastLock Auto/Manual Mode Select. When F13 HIGH, selects auto or manual FastLock mode.
F13	Out 0 (pin 21) Normal/FastLock select. When LOW the state of Out 0 (pin 21) is controlled by F8. When HIGH Out 0 is used for FastLock.
F14−F15	Power Down Mode Control. See Table III.
F16−F18	FastLock Timeout Counter. See Table IV for counter values.

Table II. Mode Select Truth Table

	F1 Pre-scaler Mod.	F2 Phase Det. polarity	F3 I_{cpo}	F4 D_o TRI-STATE	F6–F7 Power Down Modes	F8–F10 CMOS Outputs
0	32/33	Negative	LOW	Normal Operation	Powered UP	LOW
1	64/65	Positive	HIGH	TRI-STATE	Powered Down	HIGH

TABLE IIIa. Power Down Modes

Function	F15	F14
Software Control	0	0
Test Mode (See Note)	0	1
Test Mode (See Note)	1	0
Hardwire Power Down	1	1

Note: Not used in application.

TABLE IIIb. Power Control Modes

		High	Low
Software Control	F6	Receiver Off	Receiver On
	F7	Transmitter Off	Transmitter On
Hardwire Control	Rx PD	Receiver Off	Reciever On
	Tx PD	Transmitter Off	Transmitter On
	PLDD PD	PLL Off	PLL On

TABLE IV. Charge Pump Output, Out 0, and FastLock Decoding

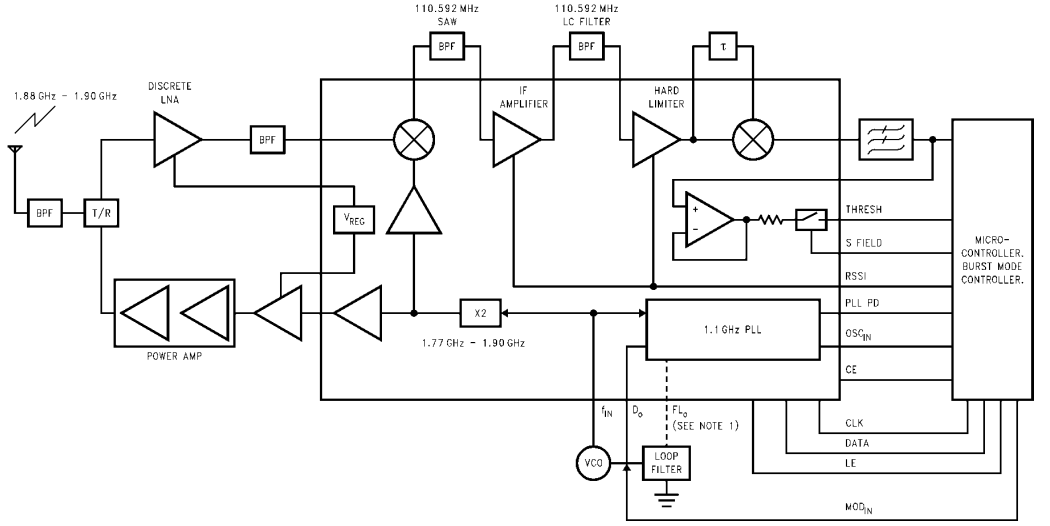
F3	F12	F13	Function
0	X	0	I_{cpo} = 1X, No FastLock, Out 0 = F8
1	X	0	I_{cpo} = 4X, No FastLock, Out 0 = F8
0	0	1	I_{cpo} = 1X, Manual FastLock, Out 0 = FL_o
1	0	1	I_{cpo} = 4X, Manual FastLock, Out 0 = FL_o
X	1	1	I_{cpo} = Set by # reference cycles present in F counter, Auto FastLock, Out 0 = FL_o

TABLE V. FastLock Timeout Counter Value Programming

Time Out (# Reference Cycles)	8	24	40	56	72	88	104	120
F16	0	1	0	1	0	1	0	1
F17	0	0	1	1	0	0	1	1
F18	0	0	0	0	1	1	1	1

Example: To set FastLock timeout for 24 reference cycles, set F16 = HIGH, F17 = LOW, and F18 = LOW.

Typical Application Block Diagram



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Note 1: Connected when using FastLock.

System: DECT—System +3V Only

		Data Per Stage			Cumulative Data				
#	Component	Gain	N Fig	OIP3	#	Gain	N Fig	IIP3	OIP3
1	Filter/Switch	−2.0	2.0	100.0	1	−2.0	2.0	97.9	95.9
2	Discrete LNA	10.0	2.0	7.0	2	8.0	4.0	−1.0	7.0
3	Filter	−2.0	2.0	100.0	3	6.0	4.2	−1.0	5.0
4	Mixer	18.0	5.9	1.0	4	24.0	5.2	−23.0	1.0
5	SAW	−11.0	11.0	100.0	5	13.0	5.3	−23.0	−10.0
6	IF Amplifier	25.0	4.0	57.0	6	38.0	5.4	−23.0	15.0
7	BPF (LC)	−2.0	2.0	100.0	7	36.0	5.4	−23.0	13.0
8	IF Limiter	60.0	18.0	68.0	8	96.0	5.4	−29.2	66.8
	SYSTEM CUMULATIVE VALUES								
	Sensitivity (@ 25°C)	−93.1 dBm			Gain	96.0 dB			
	Required Eb/No	14.0 dB			N Fig	5.4 dB			
					IIP3	−23.0 dBm			
					OIP3	66.8 dbm			

Note: Assumes 50 dB attenuation of interferer by the SAW filter and 8 dB attenuation by the LC filter.

Application Information

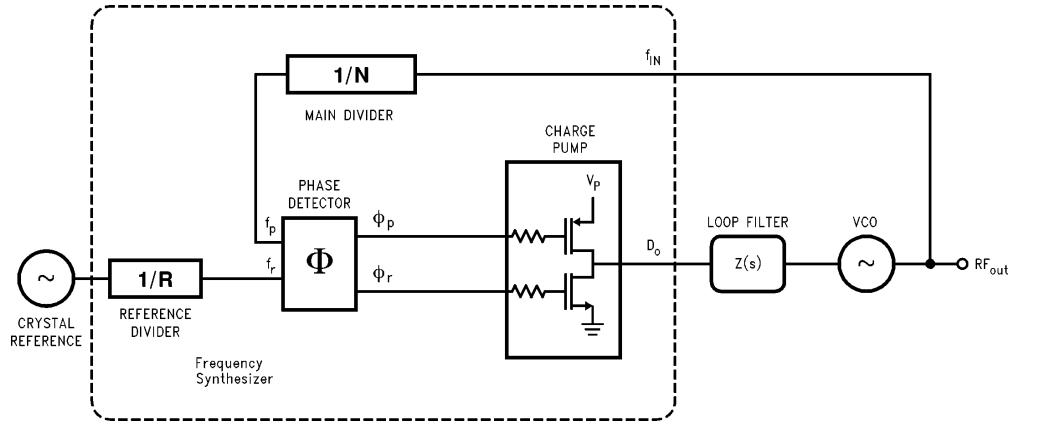

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FIGURE 1. Conventional PLL Architecture

Loop Gain Equations

A linear control system model of the phase feedback for a PLL in the locked state is shown in *Figure 2*. The open loop gain is the product of the phase comparator gain (K_ϕ), the VCO gain (K_{VCO}/s), and the loop filter gain Z(s) divided by the gain of the feedback counter modulus (N). The passive loop filter configuration used is displayed in *Figure 3*, while the complex impedance of the filter is given in *Equation 2*.

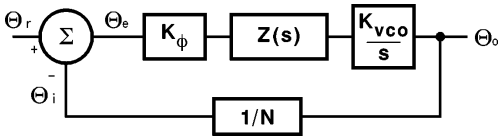

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FIGURE 2. PLL Linear Model

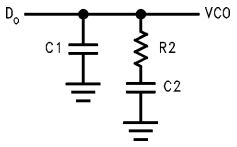

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FIGURE 3.

PASSIVE LOOP FILTER

$$\text{Open loop gain} = H(s)\,G(s) = \Theta i/\Theta e = K_\phi\,Z(s)K_{VCO}/Ns \quad (1)$$

$$Z(s) = \frac{s(C2 \bullet R2) + 1}{s^2(C1 \bullet C2 \bullet R2) + sC1 + sC2} \quad (2)$$

The time constants which determine the pole and zero frequencies of the filter transfer function can be defined as

$$T1 = R2 \bullet \frac{C1 \bullet C2}{C1 + C2} \quad (3a)$$

and

$$T2 = R2 \bullet C2 \quad (3b)$$

The 3rd order PLL Open Loop Gain can be calculated in terms of frequency, ω, the filter time constants T1 and T2, and the design constants K_ϕ, K_{VCO}, and N.

$$G(S) \bullet H(S)\Big|_{S = j\bullet\omega} \frac{-K_\phi \bullet K_{VCO}(1 + j\omega \bullet T2)}{\omega^2 C1 \bullet N(1 + j\omega \bullet T1)} \bullet \frac{T1}{T2} \quad (4)$$

From *Equation 3* we can see that the phase term will be dependent on the single pole and zero such that the phase margin is determined in *Equation 5*.

$$\phi(\omega) = \tan^{-1}(\omega \bullet T2) - \tan^{-1}(\omega \bullet T1) + 180° \quad (5)$$

A plot of the magnitude and phase of G(s)H(s) for a stable loop, is shown in *Figure 4* with a solid trace. The parameter ϕ_p shows the amount of phase margin that exists at the point the gain drops below zero (the cutoff frequency wp of the loop). In a critically damped system, the amount of phase margin would be approximately 45°.

If we were now to redefine the cut off frequency, ω_p', as double the frequency which gave us our original loop bandwidth, wp, the loop response time would be approximately halved. Because the filter attenuation at the comparison frequency also diminishes, the spurs would have increased by approximately 6 dB. In the proposed FastLock scheme, the higher spur levels and wider loop filter conditions would exist only during the initial lock-on phase—just long enough to reap the benefits of locking faster. The objective would be to open up the loop bandwidth but not introduce any additional complications or compromises related to our original design criteria. We would ideally like to momentarily shift the curve of *Figure 4* over to a different cutoff frequency, illustrated by the dotted line, without affecting the relative open loop gain and phase relationships. To maintain the same gain/phase relationship at twice the original cutoff frequency, other terms in the gain and phase equations 4 and 5 will have to compensate by the corresponding "$1/\omega$" or "$1/\omega^2$" factor. Examination of equations 3 and 5 indicates the damping resistor variable R2 could be chosen to compensate the "ω" terms for the phase margin. This implies that another resistor of equal value to R2 will need to be switched in parallel with R2 during the initial lock period. We must also insure that the magnitude of the open loop gain, H(s)G(s) is equal to zero at $\omega_p' = 2\ \omega_p$. K_{vco}, K_ϕ, N, or the net product of these terms can be changed by a factor of 4 to counteract the ω^2 term present in the denominator of *Equation 3*. The Kϕ term was chosen to complete the transformation because it can readily be switched between 1X and 4X values. This is accomplished by increasing the charge pump output current from 1.5 mA in the standard mode to 6 mA in FastLock.

FastLock Circuit Implementation

A diagram of the FastLock scheme as implemented in National Semiconductors LMX3160 is shown in *Figure 5*. When a new frequency is loaded, the charge pump circuit receives an input to deliver 4 times the normal current per unit phase error while an open drain NMOS on chip device switches in a second R2 resistor element to ground. The user calculates the loop filter component values for the normal steady state considerations. The device configuration ensures that as long as a second identical damping resistor is wired in appropriately, the loop will lock faster without any additional stability considerations to account for. Once locked on the correct frequency, the PLL will then return to standard, low noise operation. This transition does not affect the charge on the loop filter capacitors and is enacted synchronous with the charge pump output. This creates a nearly seamless change between FastLock and standard mode.

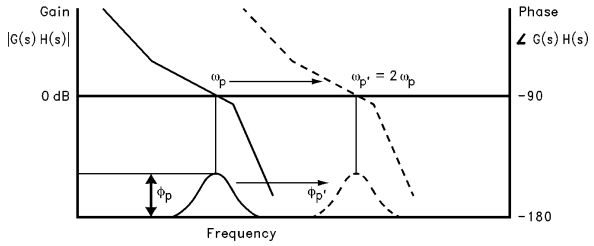

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Figure 4. Open Loop Response Bode Plot

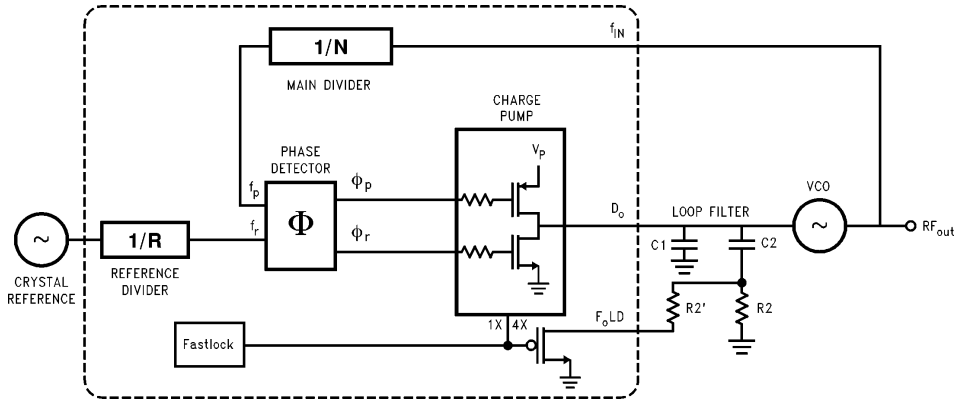

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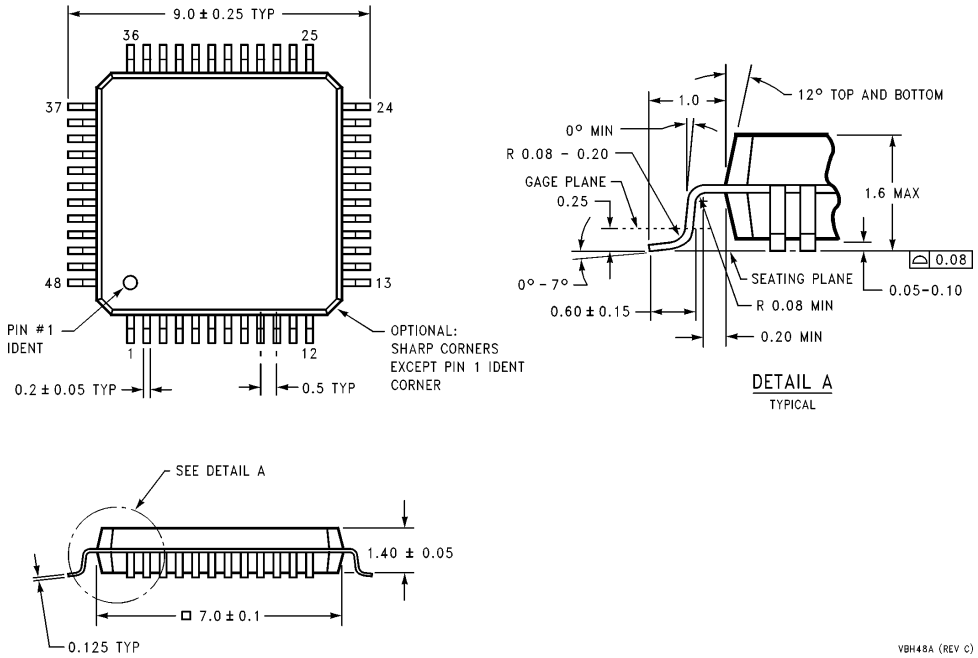
FIGURE 5. FastLock PLL Architecture

Physical Dimensions (millimeters)



48-Lead (7mm x 7mm) Molded Plastic Quad Flat Package, JEDEC
Order Number LMX3160
NS Package Number VBH48A

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