Develop A Trimless Voltage-Controlled Oscillator

Trimless VCOs, Part 2

Modeling and designing a trimless VCO requires a full understanding of the non-ideal nature of oscillator components and architectures.

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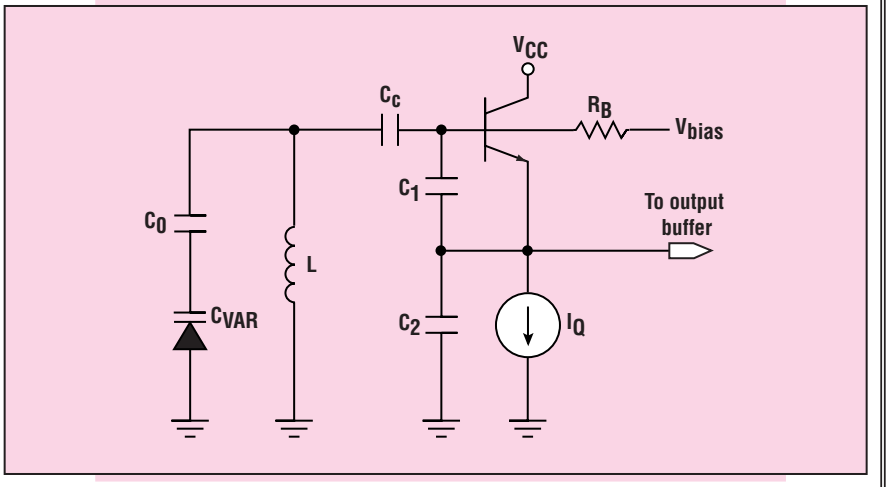
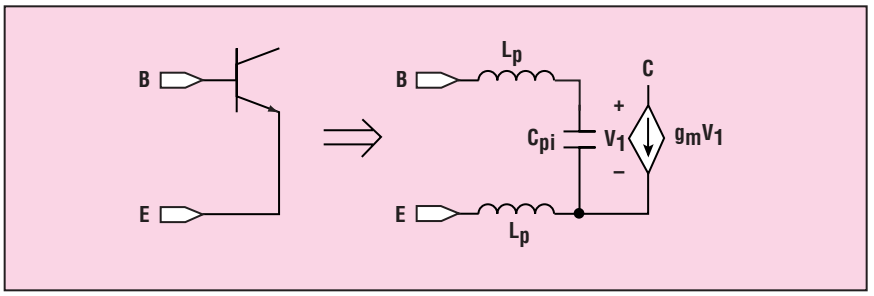
TRIMLESS voltage-controlled oscillators (VCOs) offer a practical alternative to conventional discrete VCO approaches that rely on tuning adjustments during production. The Colpitts style oscillator topology offers a proven circuit architecture for use in a trimless VCO design. A basic set of fundamental design equations can be derived for first-order oscillator design and selection of component values. Unfortunately, real-world components used to implement the trimless VCO are non-ideal and alter the governing equations. The conclusion of this two-part article on trimless VCOs covers how actual circuit implementation departs from the ideal, offering an improved method for modeling, designing, and implementing trimless VCOs.

In Part 1 (see *Microwaves & RF*, July 1999, p. 68), the Colpitts configuration (Fig. 7) was presented as the basis for a trimless VCO. The classic oscillator topology was described with a generalized set of equations to predict the fundamental oscillator behavior for the first-order design of the oscillator (i.e., component selection). The variation (error) in actual oscillation frequency was described in terms of the part-to-part errors of the frequency-setting components. The total frequency error was computed by skewing the value of each component by its worst-case tolerance. The equations proved useful in developing a table of calculations to predict the required tuning range, start-up conditions, phase noise, and



7. This VCO is based on an ideal Colpitts configuration (with a parallel-mode tank circuit).



8. This revised small-signal packaged transistor model forms the core of the new trimless VCO design.

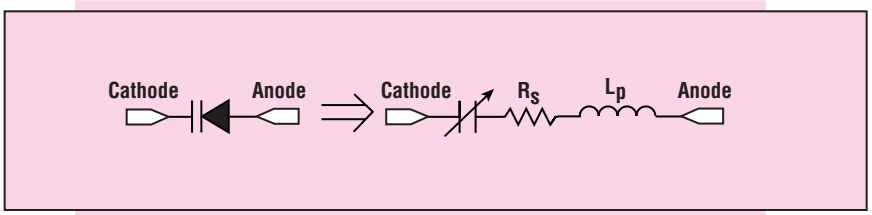
oscillation amplitude. Finally, a first-order, step-wise design process was introduced as a simple approach to select the initial component values for the Colpitts configuration with parallel-mode tank.

Although the basic theory applied in Part 1 is useful for first-order design, accurate selection of component values in a real-world oscillator requires consideration of important circuit details. The aim of this article is to present a possible approach to more accurately model the real-world equivalent of the Colpitts oscillator topology and to apply it to the trimless VCO concept. The primary objective is still to provide a simple design process that permits accurate selection of the initial component values close enough so that minimal fine tuning of the values in the actual circuit is needed to achieve oscillator operating requirements. This article will cover the effects of non-ideal components and models for them, layout parasitic elements in a VCO, a revised oscillator model, a method for trimless VCO analysis and simulation, and an example of a Colpitts oscillator that is constructed from low-cost, commercial components and the measured results for tuning range and phase noise versus predicted results.

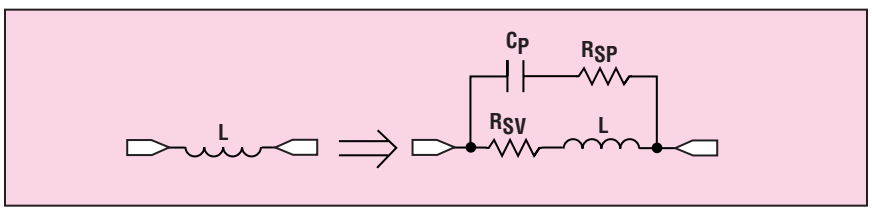
Initial analysis of the basic Colpitts configuration assumed that each component was ideal. However, when a printed-circuit-board (PCB) solution is implemented with typical surface-mount components, the real characteristics for each device must be taken into account. An examination of commonly used surface-mount components quickly reveals that they are not ideal elements, but that the elements contain amounts of parasitic resistance, capacitance, and inductance. The parasitic elements alter the frequency response of the components to the point where the effective value of the component is changed at the frequency of interest. Consequently, the oscillator frequency, tuning range, and other characteristics are affected and the real circuit departs from the operating point predicted by the first-order analysis with near-ideal components. The departure from the ideal needs to be accounted for in the design phase, in order to properly select the component values. A revised model for each component is required. The following is an examination of each component in the oscillator and a proposed circuit model for each. Again, the emphasis is on maintaining the simplest model possible in order to permit a reasonable analysis and develop some intuition in design of the oscillator circuit.

The core of a VCO is typically constructed from discrete transistors or an oscillator integrated circuit (IC). In either case, the device has finite cutoff (transition) frequency, f_T, and is typically packaged in a plastic package with metal leads (e.g., SOT-323). These factors lead to two predominate non-ideal elements in the equivalent circuit: capacitance across the base-emitter leads, and inductance in series with the base and emitter (and collector) leads of the oscillator. The capacitance results from the inherent junction capacitance and base-charging capacitance of the transistor. The full transistor circuit model would include base resistance (r_b), collector-base capacitance (C_{jc}), finite beta, etc. However, it is assumed that $f_T > f_{OSC}$, the oscillation frequency, so that r_b and C_{jc} can be considered negligible along with the other transistor parasitic elements and that the input capacitance is considered to be the dominant effect.

The inductance is a result of the parasitic bondwire and lead inductance of the package and is therefore modeled as a single lumped inductor. This lumped inductance can also include series inductance from the pin to capacitors C_1 and C_2. There are other parasitic elements, such as additional transistor parasitic elements and package shunt capacitance and mutual inductance, but their effects will be ignored for the purpose of this discussion. Figure 8 shows a revised model for the transistor that includes the parasitic capacitance (C_{pi}) and inductance (L_p). Inductance L_p is typically 1.5 to



9. This revised varactor model is employed in the new trimless VCO design for tuning purposes.



10. This revised inductor model is also part of the new trimless VCO design.

2.0 nH while capacitance C_{pi}) is typically greater than 1 pF. The base-emitter capacitance is typically greater than 1 pF for $C_{jc} + C_b$.

The parasitic capacitance, C_{pi}, and parasitic inductance, L_p, have a significant impact on the frequency response/input impedance of the active circuit amplifier. These elements must be considered and modeled to properly predict the equivalent input capacitance and negative resistance of the Colpitts oscillator configuration.

With capacitances C_1 and C_2 connected to the emitter and base leads, a revised analysis can be performed to determine the equivalent input impedance of the active circuit. For $\omega < L_pC_{pi}$, the inductor on the base side in series with C_{pi} has only a small effect on the impedance since the majority of signal current flows from the gm stage through the inductor in the emitter side. Therefore, the circuit can be simplified to facilitate analysis by including only the inductor in the emitter lead on the ideal model and provide a more intuitive approximate result. Although the majority of the signal current flows through the emitter lead, the capacitance C_{pi} should be included in the calculation of the capacitance. A reasonable approximation is $C_{1X} = C_1 + C_{pi}$. Circuit analysis shows that the inductance modifies the equivalent input impedance from the ideal model case:

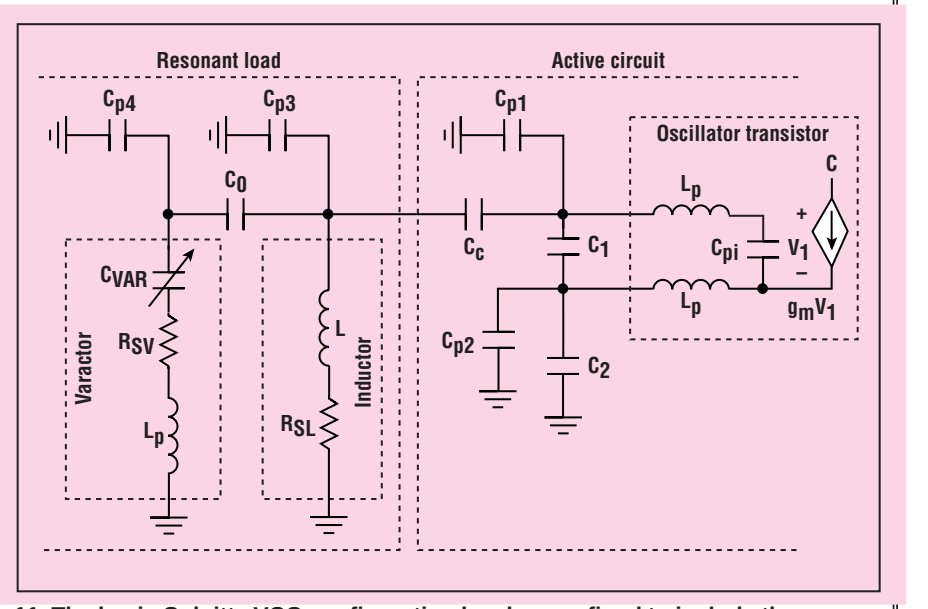
$$Z_{in} = -j[(C_1 + C_2) / wC_1C_2] + (g_m / w^2C_1C_2) \quad (14)$$

to a revised model case:

$$Z_{in} \cong -j\{[(C_{1\times} + C_2) / \omega C_{1\times}C_2] - [A / (1 + A^2)] \times (gm / \omega C_{1\times}C_2)\} + [1 / (1 + A^2)] \times (gm / \omega^2 C_{1\times} C_2) \quad (15)$$

$$where\ A = \omega g_m L_p$$

The inductor actually makes the input capacitance appear larger and the negative resistance appears smaller. The equivalent capacitance along with negative resistance may be expressed by the following equation as:



11. The basic Colpitts VCO configuration has been refined to include the realistic effects of parasitic elements.

$$C_{EQ} = 1 / \{(1 / C_{12}) - [A / (1 + A^2)] \times (gm / \omega C_{1\times}C_2)\} \quad (16)$$

and

$$-R_{EQ} = -R\left[1 / (1 + A^2)\right] \quad (17)$$

During oscillation, the current flowing in the oscillator transistor is varying versus time (typically like a half-wave rectified sine wave) and therefore the instantaneous transconductance, g_m, is varying with time. At equilibrium, the effective large-signal transconductance, G_m, is lower than the DC bias value of g_m and is only that necessary to sustain the loop gain to 1 + δ. As a result, has a reduced affect on modifying the input impedance than at its DC bias point.

One approximation which could be used for G_M is discussed in ref. 5:

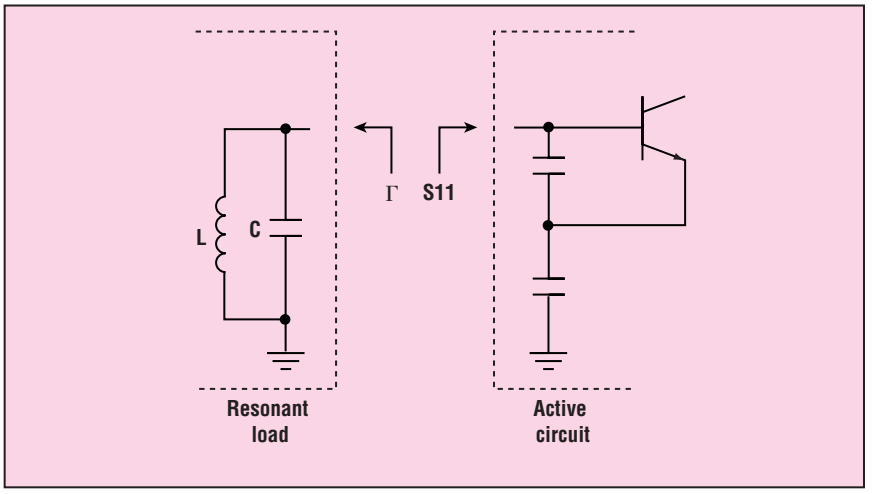
$$G_M \approx n / R_{EQ} \text{ where } n = [(C_C + C_{12}) / C_C] \times [(C_{1\times} + C_2) / C_2]$$

$$C_{12} = C_{1\times}C_2 / (C_1 + C_2) \text{ in the...} \quad (18)$$

The large-signal G_m should then be substituted for g_m in the previous equations.

Detailed simulation of the full circuit reveals that the expressions above offer a reasonable estimate of the actual equivalent input impedance. These approximations are used later to develop a revised set of design equations for the oscillator.

The varactor is essentially a positive-negative (PN) junction diode with specially tailored capacitance-versus-voltage characteristics. As with all diodes, the device has a finite static series resistance. It determines the effective capacitor and tank Q. The varactor is typically implemented as a discrete device in a plastic package (such as a SC-79 package). As with the transistor, there is a parasitic lead and bondwire inductance in series with the varactor device. These two non-ideal effects—the series inductance and the series resistance—must be included to properly predict the oscillation frequency and the tank Q (which impacts the phase noise, startup, and oscillation amplitude) In particular, the series inductance is a critical parasitic to model, because it strongly changes the effective capacitance of the varactor. (It forms a series resonant circuit that can occur very near the desired oscillation frequency.) Figure 9 shows a revised model for the varactor which includes the parasitic resistance and inductance in series with the with the anode and cathode leads. The series inductance is typically 1.5 nH while the series resistance is typically 0.5



12. This model treats an oscillator as an active circuit with a resonant load.

to 1.0 Ω.

The primary inductor in the tank circuit has a self-resonant frequency that may affect the frequency of oscillation. A relatively simple model can be used to describe the inductor below the self-resonant frequency. Figure 10 shows the revised model for the inductor. The series resistance (R_s) models the loss in the inductor that sets the Q. Capacitance (C_p) models the finite self-resonant frequency. Some manufacturers are supporting this model for their commercial devices.[6] However, many cost-effective surface-mount inductors that are available today have sufficiently high self-resonant frequencies that it is reasonable to consider the inductor to have negligible parasitic capacitance. This permits the inductor to be modeled as purely an inductance and a series resistance. The series resistance of the inductance does need to be modeled to accurately describe the tank Q.

COUPLING CAPACITORS

The feedback and coupling capacitors are high-quality RF components. Typically, the capacitors are very small (0603, 0402, even 0201) multilayer ceramic surface-mount capacitors. That technology's small size inherently provides very-high frequency performance and nearly ideal frequency characteristics. Therefore, the capacitors are considered ideal for the purposes of this second-order design.

A potentially troublesome non-ideal factor in the PCB level oscillator design has to do with the parasitic capacitances and inductances that are associated with the component solder pads and interconnect traces. These parasitic elements must be extracted from the actual PCB layout but are typically not available at the time of design, because the layout has not been started/completed. However, it is important to include them in the oscillator circuit model to accurately predict the oscillation frequency and tuning range, so a first cut layout and analysis of the parasitic element values are needed. A choice must be made between modeling the parasitic elements with transmission lines or lumped-element equivalents. Strictly speaking, the traces/pads are transmission lines, but the lumped element approach can provide a more intuitive method of modeling the parasitic elements and is valid for compact layouts where the interconnects are short (< 40 mil) and wide (>20 mil). In general, if traces are short then the connection could be approximated as just a shunt capacitance to ground. This permits the simple addition of parasitic shunt capacitors at the connection nodes. The parasitic capacitance at the connection points can be approximated by a parallel plate capacitance, C_{pad}, with the plate area equal to the total pad/trace area.

$$C_{PAD} = \varepsilon_r \varepsilon_o \times (A/t) = 1.3 \times 10^{-15} \times (A/t) pF/mil \ (for\ FR4) \qquad (19)$$

where:

A = the capacitor plate area (in square mil), and

t = the board thickness (in mil).

The active circuit negative resistance for the PCB-level oscillator design is:

$$-R_{NEQ} = -R_N\left[1/(1+A^2)\right] \qquad (20)$$

where

The resonant load capacitance can be found from:

$$A = \omega G_m L_p C_{VAREQ} = \left[C_{VAR}/(1-\omega^2 L_p C_{VAR})\right] + C_{p4} \qquad (21)$$

$$C_{VEQ} = (C_0 C_{VAREQ}/C_0 + C_{VAREQ} + C_{VAREQ}) + C_{p3} \qquad (22)$$

The resonant frequency or frequency of oscillation can be found from:

$$f_o \sim 1/\left[2\pi_{TEQ}^{0.5}\right] \qquad (23)$$

$$C_{TEQ} = C_{VEQ} + C_{IN} \qquad (24)$$

The quality factor (Q) of the resonant tank circuit, Q_T, can be found from:

$$Q_T = T_{TEQ}/2\pi L \qquad (25)$$

$$R_{TEQ} = R_{QL} \parallel R_{QC} \qquad (26)$$

$$Q_C = 1/2\pi C_V R_S \qquad (27)$$

The amplitude of the oscillation (the RMS voltage) can be found from:

with

$$R_{QC} = Q_C^2 \times R_{SC} Q_L = 2\pi L R_{SL}$$

$$R_{QL} = Q_L^2 \times R_{SL} V_O = 2 I_Q R_{EQ} \times \left[J_1(\beta)/J_0(\beta)\right] \times V_{peak} \qquad (28)$$

The loop gain can be found from:

where

$\left[J_1(\beta)/J_0(\beta)\right] \approx 0.7$ *the ratio of the Bessel functions*

$$Loop\ gain = g_m R_{EQ}(1/n) \qquad (29)$$

where

$$n \approx \left[(C_C + C_{12\times})/C_c\right] \times \left[(C_{1X} + C_{2X})/C_{2X}\right] \qquad (30)$$

The start-up criteria are given by:

$$g_m / C_1 C_2 >> R_{EQ} / Q_T^2 \quad \text{for a minimum 2:1 ratio} \qquad (31)$$

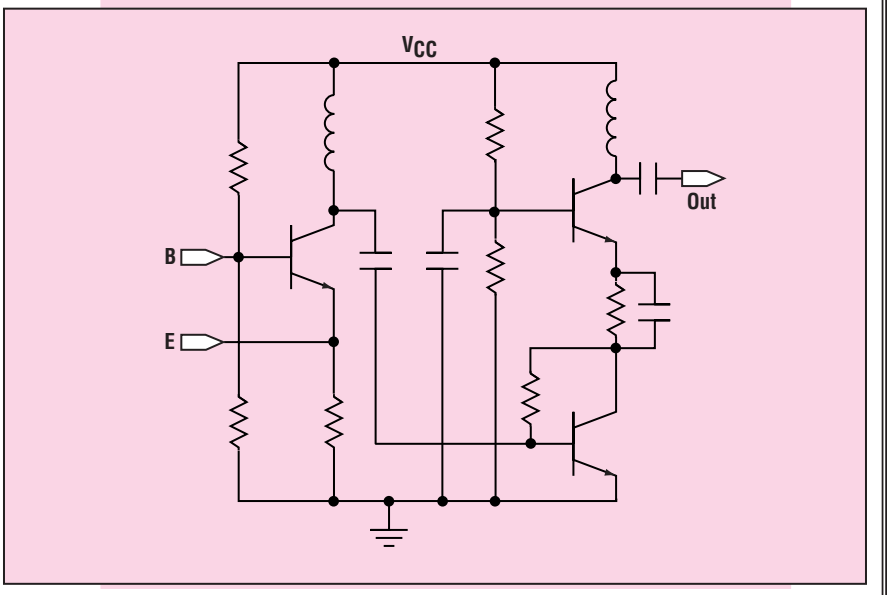
The phase noise can be found from:

$$\text{Phase noise} = I_n^2 \times (1 / V_o^2) \times (f_o / 2Q_o^2) \times \left[R_{EQ}^2 / (f - f_o^2\right] \qquad (32)$$

where:
f_o = the frequency of oscillation,
C_{VAR} = the varactor capacitance,
Q_L = the inductor quality factor,
Q_T = the tank quality factor,
R_{EQ} = the equivalent tank parallel resistance,
g_m = the oscillator bipolar transistor transconductance,
V_0 = the RMS tank voltage,
C_T = the total tank capacitance,
C_0 = the varactor coupling capacitance,
Q_V = the effective varactor quality factor,
R_S = the varactor series resistance,
I_Q = the oscillator transistor bias current, and
I_n = the collector shot noise.

One very useful method to view an oscillator circuit is as a "reflection amplifier." This intuitive concept is described in a classic article by John Boyles[7] and in a paper by Esdale.[8] The "reflection amplifier" method permits the engineer to use S-parameters for design and measurement of the oscillator. Working with S-parameters facilitates the modeling and measurement of the actual oscillator circuit and helps develop insight into the circuit's performance and potential problems.[9]

The "reflection amplifier" approach basically models the oscillator as an active circuit with a resonant load and describes the stable oscillation point in terms of the relative impedances. If the active circuit input S-parameters are plotted as $1/S_{11}$, then the values can be directly plotted on a Smith chart with the Γ of the resonant load. A convenient aspect of plotting $1/S_{11}$ is that the impedance of R and X for the active circuit can be read and multiplied by –1 to provide the correct values of the negative resistance and reactance. This method of plotting the impedances provides a graphical representation of when oscillation conditions exist.



13. This oscillator active circuit is based on the use of a discrete transistor.

The basic conditions for oscillation are:
1. $|1/S11| \le |\Gamma|$,
2. $\text{ang}(1/S11) = \text{ang}(\Gamma)$, and
3. the curves of $1/S_{11}$ and Γ must ultimately intersect each other and change in opposite angular directions versus frequency (this occurs at the peak-oscillator tank amplitude).

The reflection amplifier approach will be used in the remainder of this article to model, simulate, and measure the real oscillator circuit.

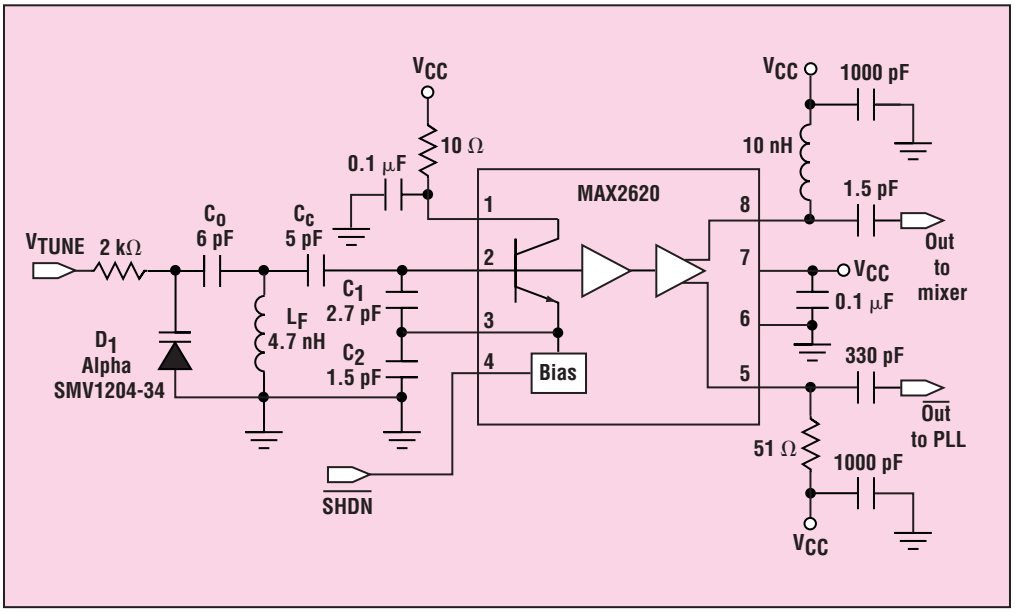
The calculations shown are valid as a method to approximate the initial values for the components. A spreadsheet can be developed to compute the revised component values (available on request from the author). It is important to view the circuit's true dependency versus frequency, start-up conditions, etc. Computer simulations should be used to provide a more rapid, accurate method of modifying the circuit component values that govern the oscillation behavior. Simulation is an efficient way to make circuit design trade-offs and adjustments to account for the changes caused by the non-ideal circuit elements.

The basic circuit model can be simulated with a small-signal circuit simulation, which inherently works in terms of S-parameters. A "small-signal" linear circuit simulation is, by far, the most rapid simulation mode available. It is best to use a commercial circuit simulator, such as the Advanced Design System (ADS) from Agilent Technologies (Santa Rosa, CA), MMICAD from Optotek (Kanata, Ontario, Canada), the Serenade Suite from Ansoft (Pittsburgh, PA), and Microwave Office from Advanced Wave Research (El Segundo, CA) for this. The simulator should be set up to use the "reflection amplifier" method that was previously mentioned, using the oscillator circuit model of Fig. 11. The initial values can be derived from the revised design equations. Adjustments can be made to the component values to return the active circuit and resonant load impedances back to the values required for the desired oscillation frequency, start-up, and tuning range. In some cases, the values predicted by the small-signal circuit model are a sufficient and accurate estimation of the component values to proceed directly toward constructing the actual circuit (Fig. 12). However, when a more accurate or highly optimized design is required, it may be necessary to simulate the actual active circuit implementation with detailed models for all devices. The full oscillator circuit is then simulated with a time-domain simulator (e.g., SPICE) or a harmonic-balance simulator (e.g., Harmonica) to precisely determine the frequency tun-

ing range and verify that the circuit design objectives can be met.

EXAMPLE CIRCUIT

Implementation of the Colpitts configuration shown in Fig. 7 is commonly accomplished with discrete transistors. Many options exist for cost-effective, high f_T transistors packaged in small plastic packages—as single and dual devices. However, in order to achieve a design that works down to a +2.7-VDC supply voltage with sufficient headroom for the oscillator device and output buffer, a three-transistor circuit is typically needed. Figure 13 shows the possible implementation of the oscillator active circuitry.



14. Based on a model MAX2620 oscillator IC, this design represents a practical implementation of the Colpitts oscillator configuration.

Discrete implementations are extremely flexible, but possess several negatives. The primary negatives of this circuit are significant variation in biasing versus temperature and supply voltage, the large number of components required to implement the oscillator active circuitry, and the relatively large PCB area that is required.

An improved alternative to the discrete transistor approach is to use an integrated oscillator IC, such as the MAX2620 from Maxim Integrated Products (Sunnyvale, CA), with an external tank circuit. The MAX2620 IC integrates the oscillator transistor, stable biasing, and an output amplifier in a small uMAX8 package to provide a convenient method of implementing the oscillator active circuitry.[10] This approach permits the designer to focus only on selecting the external passive component values, thereby confining the design task to achieve the required frequency tuning characteristics. Figure 14 shows the Colpitts oscillator configuration using the MAX2620. The frequency-setting components are all on the left side of the circuit. The components that are connected to the output ports are one possible option to implement the output matching to the load.

Referring to the revised circuit model of Fig. 11, the parasitic-element values in the component models are as follows. For the varactor, L_p = 1.5 nH, R_{sv} = 0.5 Ω, C_{var}(hi) = 8 pF, and C_{var}(lo) = 4 pF. For the inductor, L_p = 4.7 nH and R_{sl} = 0.5 Ω. For the transistor, L_p ~ 3.0 nH and Cpi = 1.1 pF. For the layout parasitics, C_{p1} = 0.2 pF, C_{p2} = 0.2 pF, C_{p3} = 0.5 pF, C_{p4} = 0.3 pF, and L_{trace} = 0.3 nH.

The component values are selected through a simple design process that is summarized below as part of the revised design process:

- Select initial values for C_1, C_2, L_f, C_c, C_o, C_{var}(hi), and C_{var}(lo) based on the revised design equations developed for C_{var}, C_v, C_{in}, and C_{12e} described in this article to achieve the require frequency tuning range required for the trimless VCO.
- Construct a more detailed small-signal circuit model using the revised models for the varactor, active circuit, and layout parasitic elements.
- Simulate the small-signal circuit model and adjust the component value to achieve the target values for C_{in}, $C_{var(hi)}$, $C_{var(lo)}$, and startup conditions (maintain loop gain and sufficient negative resistance).
- Construct the oscillator with the simulated component values.
- Measure $1/S_{11}$ and Γ (optional).
- If any fine-tuning frequency adjustment is necessary, adjust the frequency of oscillation with C_o, C_c (for an increase in frequency, decrease C_c and for a decrease in frequency, increase C_c; increase the tuning range and decrease the frequency by increasing C_o; and decrease the tuning until the tuning range and frequency limits match a particular set of requirements).

A circuit (Fig. 14) was constructed in prototype fashion to demonstrate the performance of an oscillator designed from the equations and simulation technique outlined in this article. The circuit is useful for some commercial 900-MHz industrial-scientific-medical (ISM) applications. ●●

Acknowledgments

The author would like to acknowledge that there are many previous contributors to the field of oscillators that are the respected experts (Rohde, Leeson, Boyles, Hayward, Meyer, etc.). Their work has led to the advancement of oscillators in general and provided the foundation for this two-part article. My effort was simply to introduce a simple concept for a trimless VCO and to re-describe the oscillator design task in a simple, improved manner in order to permit an engineer to quickly calculate the initial component values for a PCB-based Colpitts VCO design.

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