Low-Noise Local Oscillator Design Techniques using a DLL-based Frequency Multiplier for Wireless Applications

by

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Abstract

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University of California, Berkeley

Professor Paul R. Gray, Chair

The fast growing demand of wireless communications for voice and data has driven recent efforts to dramatically increase the levels of integration in RF transceivers. One approach to this challenge is to implement all the RF functions in the low-cost CMOS technology, so that RF and baseband sections can be combined in a single chip. This in turn dictates an integrated CMOS implementation of the local oscillators with the same or even better phase noise performance than its discrete counterpart, generally a difficult task using conventional approaches with the available low-Q integrated inductors. This is a particularly severe problem in RF systems such as AMPS, where the channel spacing is small and close-in phase noise must be extremely low.

In this thesis the fundamental performance limit of a local oscillator design using a DLL-based frequency multiplier is investigated. The distinctive timing jitter accumulation pattern of a DLL-based frequency multiplier is analyzed in detail to predict the phase noise performance based on the thermal-noise-induced jitter of the source-coupled differential CMOS delay cell implementation. The result suggests an unique phase noise signature compared to a PLL approach using a VCO. Due to the limited timing jitter

accumulation in a DLL, the close-in phase noise performance of the DLL-based frequency multiplier is much lower than that of a monolithic VCO.

The specific research contributions of this work include (1) proposing a new local oscillator architecture using a DLL-based frequency multiplier that breaks the traditional LO phase noise limitations, (2) an analytical model that describes the phase noise performance of the proposed local oscillator architecture, (3) the application of the DLL-based frequency multiplier to a monolithic CMOS low-phase-noise local oscillator for cellular telephone applications.

To demonstrate the proposed concept, a fully integrated CMOS local oscillator utilizing a DLL-based frequency multiplier technique to synthesize a 900MHz carrier with low close-in phase noise was designed. This prototype, implemented in a standard 0.35μm CMOS technology, achieves -123dBc/Hz phase noise at 60kHz offset while dissipating 130mW from a 3.3V supply, meeting the requirements of the IS-137 dual-mode standard.

Approved By:

Paul R. Gray, Committee Chair

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Chapter 1

Introduction

1.1 Motivation

The market for wireless communication has grown explosively in recent years with the fast development of new products and services. Current devices on the market, such as cordless/cellular telephones, wireless LAN's, and GPS/satellite receivers, utilize the frequency spectrum between 800 *MHz* to 2.5 *GHz* for communication. As technology advances, today's savvy consumers demand wireless systems that are low-cost, low-power and with a small form-factor. Therefore, much recent effort in circuit design for wireless systems has been devoted to the design of a single-chip transceiver implemented in the low-cost CMOS technology [1][2]. This requires researches in new transceiver architectures and circuit design techniques that will enable a fully integrated RF transceiver. One of the key components in the integrated RF transceiver is the frequency synthesizer, whose main functions are to provide a precise carrier frequency for the local oscillator and to supply the accurate timing information for the sampling circuits in baseband (i.e., switched capacitor filter and analog-to-digital converter). This dissertation focuses on the new

design technique of a DLL-based frequency multiplier that is used as the local oscillator for wireless applications.

To achieve optimal system performance, the following two factors are essential: precise frequency generation for local oscillators in communication systems, and accurate timing-edge generation for sampled-data circuits in baseband. For most communication systems, a reference crystal oscillator either provides the required timing information or functions as a reference for a frequency synthesis block, such as a Phase-Locked Loop. Therefore, minimizing the *additive* timing error (noise introduced in the active circuit block) is the primary task in the design. In some systems, timing information and data are recovered from a corrupted signal (for example, local area network, ADSL, fiber-optic link, etc. [3][4][5]); in this case, low-jitter timing generation is desirable.

Two main types of timing uncertainties are critical in communication systems: timing jitter and spurious tones. Timing jitter is the random timing fluctuation of clock edges in the time domain. In a sampled-data application, random timing fluctuation affects the timing accuracy of the sampled data. Spurious tones are periodic timing fluctuations of clock edges in the time domain. In a wireless transmitter application, spurious tones in a local oscillator create undesired spectral emissions at undesired frequencies. Many sources of errors that are present in actual implementations of the system may also affect the timing uncertainties, including supply variation, substrate coupling, etc.

In most wireless communication systems, information is modulated and transmitted at a much higher frequency than the signal bandwidth, commonly known as the carrier frequency. A precise frequency synthesizer, usually implemented with a *Phase-Locked Loop* (PLL), is used to generate the carrier frequency. To maximize the spectral usage and optimize performance within the available bandwidth, timing uncertainties (both random and periodic) need to be minimized. Conventionally, the *Voltage-Controlled Oscillator* (VCO) in a PLL is implemented with an external resonator, such as a LC-tank. An external resonator is generally of very high quality, which minimizes noise contributions. However, with the reduction of the external component count and an increasing level of integration for RF transceivers, the selectivity and sensitivity are often compromised by using integrated VCOs.

Already present in today's clock/data recovery systems (such as disk drive read channels and 10/100Base-T LAN applications), an on-chip ring-oscillator [6] and a voltage-controlled delay line [7][8][9] have resulted in a higher integration and lower cost solution than discrete component implementations. An increasing number of research publications employ various VCO and synthesizer design techniques to target radio applications [6][10][11][12][13][14]. However, because the phase noise requirement of wireless systems is generally more difficult to achieve, integrated VCOs and synthesizers may not be useful for RF frequency synthesis without new design techniques that improve their performance.

1.2 Research Goals

This research addresses the issues regarding the local oscillator integration in CMOS for wireless applications, and investigates the use of a DLL-based frequency multiplier as a local oscillator to avoid the timing jitter accumulation in oscillators. Detailed analysis is given to estimate the phase noise performance of the DLL-based frequency multiplier; in addition, CMOS design techniques of the local oscillator are also presented. For demonstration purposes, an experimental prototype based on the analysis of this research is designed to meet the specification of IS-137 cellular telephone standard [15]. This system, commonly known as the AMPS/TDMA system, is widely available throughout the world. Due to the narrow channel spacing of 30kHz, this standard represents one of the more difficult phase noise specifications in wireless systems.

The key contributions of this work are:

1. A DLL-based frequency multiplier whose timing jitter does not accumulate from cycle-to-cycle, and whose noise performance is independent of the low quality factor of on-chip spiral inductors.

2. An analytical model that describes the timing jitter and phase noise performance of the DLL-based frequency multiplier, taking into consideration the thermal-noise-induced jitter performance of CMOS differential source-coupled delay cells with PMOS triode-region loads.

3. The application of the DLL-based frequency multiplier analysis to a monolithic CMOS low-phase-noise local oscillator for cellular telephone applications.

4. Experimental results for the DLL-based frequency multiplier local oscillator fabricated in a 0.35μm double-poly 5-metal CMOS process, which show a very good agreement with the analytical predictions for phase noise and spurious tones.

1.3 Thesis Organization

Chapter 2 begins with a review of receiver and transmitter architectures. In particular, several integration-friendly architectures are discussed in detail with design trade-offs for different functional blocks. The role of frequency synthesizers in wireless communication systems for both receivers and transmitters is then introduced. The two key non-idealities for frequency synthesizers, namely *phase noise* and *spurious tones*, are discussed with their impacts on receiver and transmitter performance.

Chapter 3 begins with a brief review of Phase-Locked Loop (PLL) fundamentals as well as the key design equations of a PLL, followed by an overview of recent publications on integrated Voltage-Controlled Oscillators (VCO). This chapter concludes with a proposal of a new local oscillator architecture that addresses the two main issues that limit the performance of monolithic VCO implementations.

Chapter 4 introduces the basic operation of the DLL-based frequency multiplier and the concept to achieve low phase noise performance. Phase noise, caused by thermal-noise-induced timing error in delay cells, is carefully studied, and a mathematical model that characterizes the noise behavior is presented. Spurious tones, mainly due to mismatch

in design, are also studied. These characteristics are taken into consideration in wireless system designs.

Chapters 5 and 6 detail the implementation specifics for the DLL-based frequency multiplier block transfer function, system equation, circuit design and prototype implementation. This is followed by Chapter 7 which presents the target application and measurement results. Finally, the conclusions are presented in Chapter 8.

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Chapter 2

Frequency Synthesizer in Wireless Communication Systems

2.1 Introduction

There are many different types of wireless communication systems on the market today, ranging from cordless and cellular telephones for voice to wireless local area network for data. A sample list of existing wireless communication systems is shown in Table 2-1 along with their key parameters. Although these systems differ from each other in many different ways (i.e. carrier frequency, channel spacing, modulation format, etc.), they all contain a RF functional block to modulate and demodulate the transmitted and received signals.

Different from the “wired” communication counterpart, all wireless applications have two common characteristics: they share the same medium - electromagnetic waves through the air interface - and they all operate in a passband around a carrier frequency. The carrier frequency of recently developed wireless applications tend to increase as the spectrum becomes more crowded. The electromagnetic wave received by antennas consists of many signals for different applications (including broadcasting radio and TV chan-

TABLE 2-1 Summary of Wireless Communication Standards

Parameter	AMPS	IS-54	GSM	DECT	802.11
Origin	EIA/TIA	EIA/TIA	ETSI	ETSI	IEEE
Access	FDD	FDM/FDD/TDM	FDM/FDD/TDM	FDM/TDM/TDD	FH/FDM
Modulation	FM	$\pi/4$ QPSK	GMSK, diff	GFSK	(G)FSK
Data Rate / Channel	n/a	48 kb/sec (2 bits/symbol)	270.8 kb/sec	1.152 Mb/sec	1-2 Mb/sec
RF Channel Frequency	824-848MHz(Tx) 869-893MHz(Rx)	824-848MHz(Tx) 869-893MHz(Rx)	890-915MHz(Tx) 935-960MHz(Rx)	0:1897.344MHz 9:1881.792MHz	2.4-2.5GHz
Number of RF Channels	833	833	124	10	75
Channel Spacing	30kHz	30kHz	200kHz	1.782MHz	1MHz

nels, military information, aeronautical and maritime communication). For the wireless *receiver*, the desired information is only a very small part of this broad spectrum of received signal; as a result, it is inherently difficult to extract the desired information. To maximize the bandwidth usage, higher carrier frequencies and more stringent spectrum restrictions to prevent interference among different wireless applications are used. At the other end, the wireless *transmitter* processes only the desired information and transmits that at RF frequency; therefore, its specification is much more relaxed.

The receiver's RF block is generally characterized by its sensitivity and selectivity. Sensitivity is a measure of the smallest input signal the RF receiver can detect while maintaining a minimum Signal-to-Noise Ratio (SNR) for a given Bit-Error-Rate (BER). Selectivity refers to the receiver's ability to demodulate a weak desired signal with a given BER in the presence of large adjacent-channel signals. Although sensitivity is primarily determined by the noise performance of the RF front-end circuits, and selectivity is largely affected by the channel select filter at IF or baseband circuits, both performance measure-

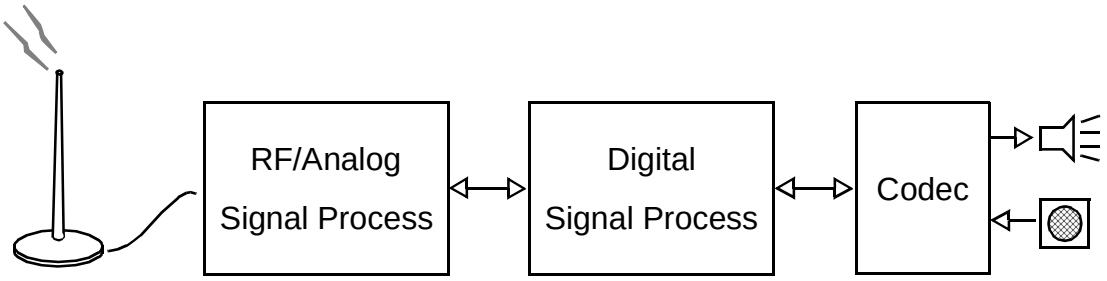

Fig. 2.1: Conceptual Block Diagram for Wireless Transceiver.

ments are also influenced by the quality of the frequency synthesizer. This chapter begins with a review of receiver and transmitter architectures with an emphasis on integration, followed by a discussion of the impact of frequency synthesizers' non-idealities on the receiver and transmitter architectures. Examples of commercial standards are given for illustration.

2.2 Receiver Architecture

Fig. 2.1 shows a conceptual block diagram of a transceiver for a cordless or cellular telephone. In the receive path, the RF signal is first received at the antenna and then passed through a series of RF/analog signal processing functions in which the RF signal is down-converted, amplified, filtered and digitized. The digital output is then processed by the Digital Signal Processing (DSP) block which may include digital filtering, demodulation, and error correction. The codec accepts the DSP output and drives an ear piece or speaker on the telephone.

Since the receiver design is inherently more difficult, this section will focus on the receive path of the RF/Analog Signal Processing block. Several different receiver architectures exist today and can be categorized into four distinct groups: *Superheterodyne*, *Direct Conversion*, *Low-IF* and *Wideband IF with Double Conversion*. Later sub-sections describe the characteristics of each architecture and their impacts on the receiver performance. Most importantly, the potential of each receiver architecture for integration will be presented.

2.2.1 Superheterodyne

The most commonly used receiver architecture today is the *Superheterodyne* architecture. This architecture was first proposed by E. H. Armstrong in 1917 (U.S. Patent) [16]; because of its superior performance, it has been widely used in various different types of radio applications. Fig. 2.2 shows a simplified block diagram of the superheterodyne receiver.

In the superheterodyne receiver architecture, the received RF signal is first passed through the external RF filter which attenuates the out-of-band blocker signals. Then the RF signal is amplified by the Low Noise Amplifier (LNA). It is important to amplify the RF signal at an early stage to increase the signal level and to minimize the impact of noise contributions from later circuit blocks. The amplified signal is then passed through an external Image Reject (IR) filter, typically one with the same characteristics as the RF filter, to further attenuate out-of-band signal and noise, in particular the signal energy in the image band[1]. The first local oscillator (LO) is a variable frequency synthesizer which gen-

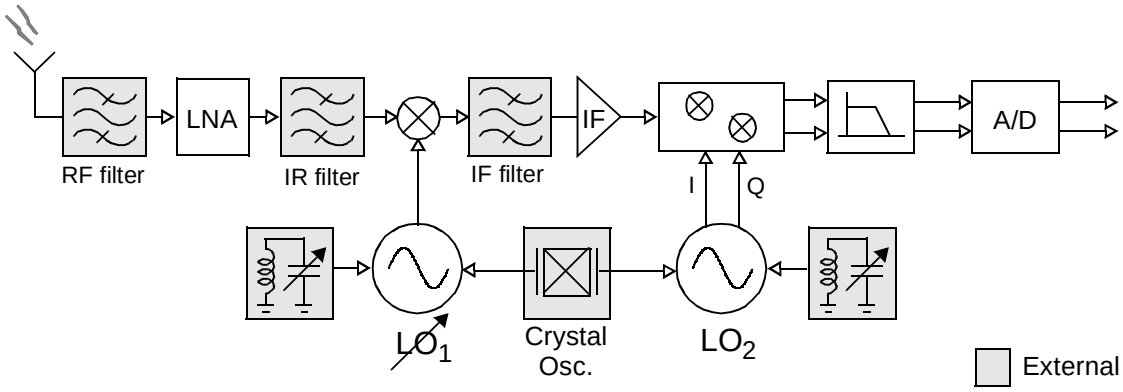

Fig. 2.2: Superheterodyne Receiver Block Diagram.

erates a channel-select RF frequency. Together with the first mixer, the first LO down-converts the desired RF channel frequency to a fixed Intermediate Frequency (IF).

The IF signal then goes through an external high-Q channel-select bandpass filter (IF Filter) which rejects most of the adjacent-channel energy and passes the desired channel to an IF amplifier. The second local oscillator generates a fixed IF frequency and down-converts the desired channel at IF to baseband with the second mixer. At baseband, the desired channel goes through the final analog signal processing which may include filtering, phase compensation, equalization and digitalization.

This architecture enjoys an excellent sensitivity and selectivity performance due to the presence of discrete high-Q filters. The RF and IR filters significantly reduce the unwanted signal energy from the image band that would potentially degrade the sensitiv-

1. After down conversion, the image band signal energy coincides with the desired signal energy, degrading the Signal-to-Noise Ratio (SNR). Careful choice of IF frequency ensures sufficient attenuation in the image band by both RF and Image Filters.

ity. The high-Q channel-select bandpass filter attenuates the adjacent channel energy and increases the selectivity performance by orders of magnitude. However, these external filters are expensive and prohibit the full integration of the receiver.

From the frequency synthesizer point of view, the first local oscillator generates a channel-select RF frequency which is required to synthesize channel frequencies in small frequency steps. Because of the loop dynamics, this frequency synthesizer needs to have a small loop bandwidth which does not provide the VCO phase noise suppression (will be discussed in detail in Chapter 3). In the superheterodyne receiver architecture, the VCO is generally implemented with high-Q external components which provides excellent phase noise performance. However, using external components prevents full integration of receiver. Recent examples of superheterodyne designs can be found in [17][18][19][20].

2.2.2 Direct Conversion (Zero-IF)

One step toward full receiver integration would be to remove the external high-Q filters that are present in the superheterodyne architecture. Shown in Fig. 2.3 is the conceptual block diagram of the *Direct Conversion* receiver architecture (also known as Zero-IF or ZIF architecture). It consists of only one external RF filter in the receive path. This receiver topology is commonly used in pager or two-way radio applications where the performance requirement is relaxed. A recent publication suggests that this architecture can also be used for cordless telephone applications with moderate performance requirements [21].

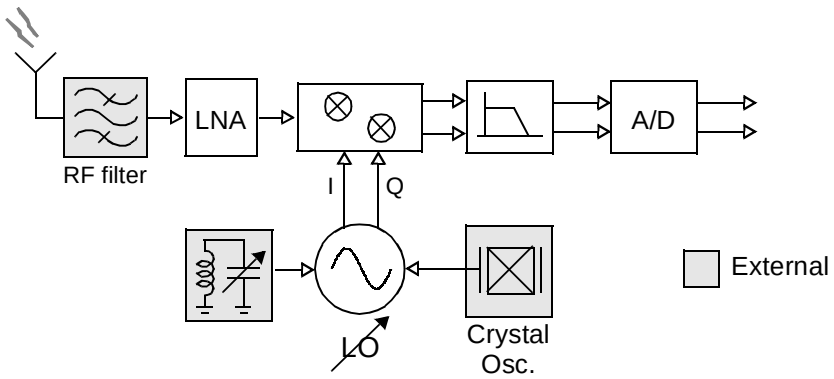

Fig. 2.3: Direct Conversion Receiver Block Diagram.

As in the superheterodyne architecture, the received RF signal is first filtered by the RF filter which attenuates the out-of-band blocker signals, and then the signal is amplified by a LNA. The local oscillator is a variable frequency synthesizer whose output is centered at the desired channel frequency. Together with the mixer, the LO signal down-converts the RF signal directly to baseband with the desired channel located at DC. Due to the direct conversion of RF signal, no image band is present; this eliminates the need for the IR filter in the superheterodyne architecture. In addition, no external IF filter is required since there is no IF frequency. At baseband, the signal is then amplified and filtered by continuous time filters and digitized by an Analog-to-Digital Converter (ADC) for further Digital Signal Processing (DSP).

In the direct conversion receiver, prior to the input of baseband circuits, the only filter present is the RF filter which attenuates energy from out-of-band RF signals. Adjacent channel energy relative to the desired channel remains unchanged at the baseband input. Since the channel-select IF filter has been removed from the receive path for integration,

the possible presence of the large adjacent channel energy with a small desired channel signal translates to a stringent linearity requirement for the baseband filter and ADC circuits [22][23]. Therefore, the sensitivity and selectivity performance of a direct conversion receiver largely depends on the design complexity of the RF and baseband circuit blocks.

In addition to the adjacent channel energy problem, other system non-idealities need to be overcome to achieve full integration. Two error sources contribute to the DC offset in the receive path. First, the local oscillator output in the direct conversion receiver centers at the desired channel frequency. A small amount of LO energy may be radiated and then received by the antenna, and it can be self-mixed down to baseband as a DC component. Due to the nature of direct conversion receiver where the gain in front of baseband is limited, the DC offset due to LO leakage can be much larger than the desired channel energy, hence saturating the desired signal. Secondly, the limited gain before the baseband circuits increases the offset requirement of later circuit blocks. As a result, the DC offsets, along with other error sources (i.e. 1/f noise) must be removed with careful circuit design techniques or an adaptive feedback system.

As in the superheterodyne receiver, the local oscillator generates a RF frequency which needs to increment in small frequency steps. In order to achieve low noise performance with a small PLL bandwidth, an external VCO is commonly used. This prohibits the full integration of the receiver.

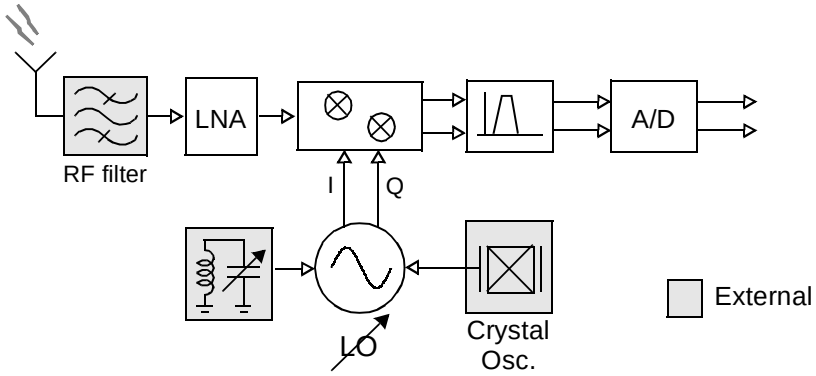

Fig. 2.4: Low-IF Receiver Block Diagram.

2.2.3 Low-IF Architecture

One way to avoid the DC offset and 1/f noise problems in the direct conversion or ZIF receiver is to place the down-converted signal away from DC. Shown in Fig. 2.4 is the block diagram for a *Low-IF* receiver topology. The RF section is identical to the ZIF receiver where no discrete filter, except the RF filter, is used in the receive path. The local oscillator frequency is deliberately selected to be slightly away from the desired channel frequency, so the down-converted desired channel will be centered at a frequency that is equal to the difference between the frequencies of the local oscillator and the desired channel. An integrated bandpass filter can be used at this frequency to perform channel selection.

This topology eliminates the DC offset and 1/f noise problems of the direct conversion architecture by down-converting the desired signal to a frequency away from DC. However, in addition to the integrated RF channel-select frequency synthesizer issue mentioned in previous two architecture examples, the low-IF topology needs to reject close-in

image energy. The down-converted desired channel is typically above DC, but low enough to ease the implementation of baseband bandpass filter. However, this creates a new problem of rejecting nearby image energy (typically a few hundred *kHz* away), much closer than the image rejection band in a conventional superheterodyne receiver (typically tens of *MHz* away). The conventional image band is strongly attenuated by the RF and IR filters in the superheterodyne receiver architecture, reducing its effect on the receiver performance. Because the nearby image energy in the Low-IF receiver cannot be filtered by the front-end RF filter, active image reject mixer techniques are required for this architecture [24]. However, active image reject mixers generally achieve a limited image rejection due to local oscillator I/Q phase and gain mismatches. Similar to the nearby image energy issue mentioned above, the specified blocker energy can also be down-converted to a frequency closer to the desired channel than the original blocker location. This increases the difficulty of designing the channel-select filter. Furthermore, the complexity of the integrated bandpass filter increases as the channel bandwidth increases due to the additional poles and zeros needed to implement the bandpass filter function versus lowpass filtering. Also, the power dissipation required for a wide bandwidth may prohibit a full integration. Therefore, because of the nearby image and blocker energy, and integrated bandpass filter issues, the low-IF architecture is suitable only for communication systems where the nearby image and blocker energy is small and the channel bandwidth is relatively narrow. An example of a low-IF receiver can be found in [25].

2.2.4 Block-Down Conversion: Wideband IF with Double Conversion

The three receiver architectures above all use a RF frequency synthesizer to perform the channel selection function. This requires the frequency synthesizer to generate LO frequencies in small frequency steps corresponding to the channel bandwidth. Due to the limitation of PLL transfer functions, this implementation requires high-Q external VCOs to achieve the required noise performance for wireless communication systems. One technique which may enable a fully-integrated receiver architectures is block down-conversion.

Block down-conversion technique utilizes a fixed-frequency first local oscillator (LO_1) to down-convert the entire RF band to IF. This technique may potentially eliminate the need for discrete IR and IF filters in the superheterodyne architecture, and allows new explorations of low-noise LO_1 design that only needs to generate a fixed frequency. One example for this approach is the *Wide-band IF with Double Conversion* (WBIFDC). This architecture also addresses some of the issues mentioned in previous sections.

Shown in Fig. 2.5 is a simplified block diagram for WBIFDC [26][27]. This topology requires no external components in the receive path, with the exception of the RF filter to attenuate out-of-band signals. It employs active image-reject mixers to reduce the image band energy. DC offset caused by LO self-mixing is eliminated by using two LO's centered at frequencies different from the carrier frequency.

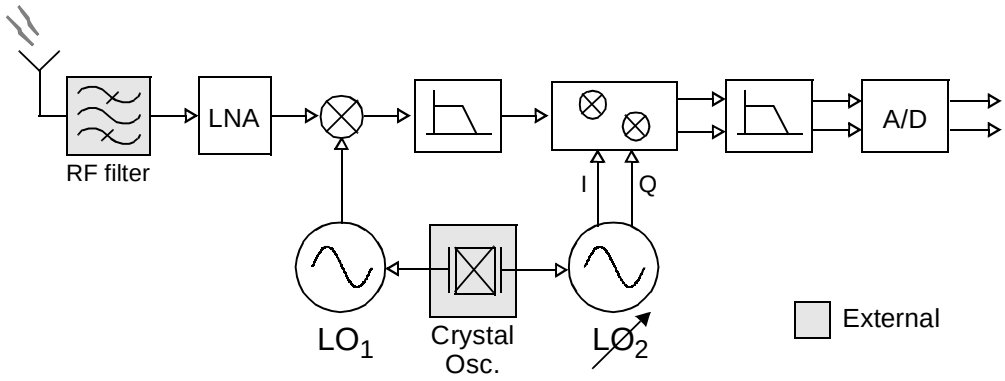

Fig. 2.5: Wideband IF with Double Conversion Receiver Block Diagram.

The received RF signal is first filtered by the RF filter and amplified by the LNA. Together with the first *fixed-frequency* local oscillator, the mixer down converts the entire received RF signal to an IF frequency where a simple RC lowpass filter attenuates higher order terms due to mixing. The second set of mixers, together with the second local oscillator tuned to the desired channel frequency at IF, down-converts the desired channel to DC for channel select filtering and digitalization. Since no discrete filter is present in the receive path for this topology, and the LO_1 is a fixed frequency synthesizer, the received signal remains wideband at the IF frequency (i.e., all the channels are present at IF). Hence, the name: wide-band IF is selected versus narrow-band at IF for the superheterodyne receiver architecture with the discrete IF filter.

With the double conversion, the image band energy is attenuated first by the RF filter and canceled by the active image reject mixers. The DC offset caused by LO leakage is eliminated with the double conversion. However, similar to the ZIF architecture, the adjacent channel energy relative to the desired channel energy is unchanged throughout the RF

section of the receiver, and this limits the linearity of the baseband section [22][23]. Also, the active IR technique is subject to the I/Q gain and phase mismatches. Therefore, the sensitivity and selectivity performance of this topology strongly depend on the design complexity of the RF and baseband circuit blocks.

One key advantage of this architecture over the previous ones is that the first local oscillator is a fixed frequency synthesizer. For reasons which will be discussed in Chapter 3, this key advantage allows the PLL bandwidth to be optimized to reduce the phase noise. This enables the full integration of the frequency synthesizer, including monolithic VCOs. Although the second local oscillator is still required to be a variable frequency synthesizer tuned to the desired channel frequency, the center frequency is at a much lower frequency, inherently providing a better phase noise performance. Because it does not have discrete filters and because the frequency synthesizer is integrated, this architecture makes possible a single-chip CMOS RF receiver [26][27][28].

2.3 Transmitter Architecture

In contrast to RF receivers, RF transmitters accept baseband information (either digital or analog) and perform RF/analog signal processing to transmit the information at the carrier frequency through the antenna. Fig. 2.6 is the functional block diagram of a transmitter. The transmitter performs modulation, up-conversion and power amplification. The baseband signal is first conditioned by baseband signal pro-

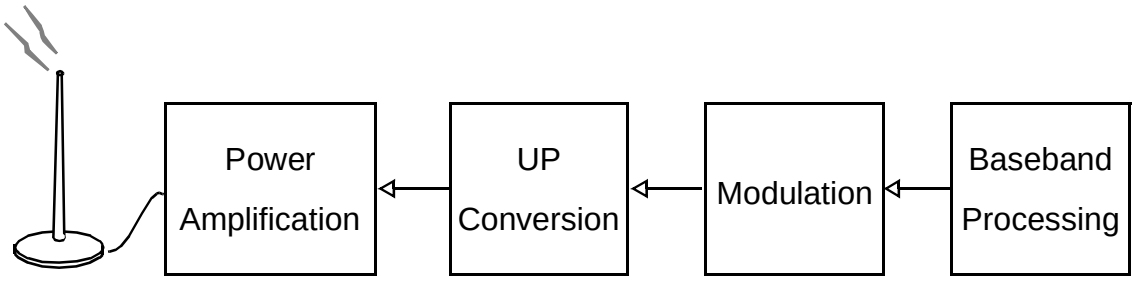

Fig. 2.6: Functional Block Diagram for Wireless Transmitter.

cessing to eliminate the unwanted information in the signal spectrum. Depending on the modulation scheme for the wireless standard, the modulation and up-conversion can be combined. The up-converted signal is power-amplified for transmission through the antenna.

Sensitivity and selectivity specifications in a transmitter are more relaxed than for receivers because the input signal is generally a band-limited baseband signal; distortion and intermodulation are the important specifications. In this section, a survey of typical transmitter architectures is presented, including the *direct conversion*, *double conversion* and *PLL* architectures. The discussions emphasize the relative merits of each architecture, their integrability and frequency synthesizer requirements.

2.3.1 Direct Conversion Transmitter

The most straightforward method to up-convert the modulated baseband information to RF is through direct conversion. Fig. 2.7 shows a block diagram of a *Direct Conversion* transmitter where the channel-select LO frequency equals the carrier frequency. The digi-

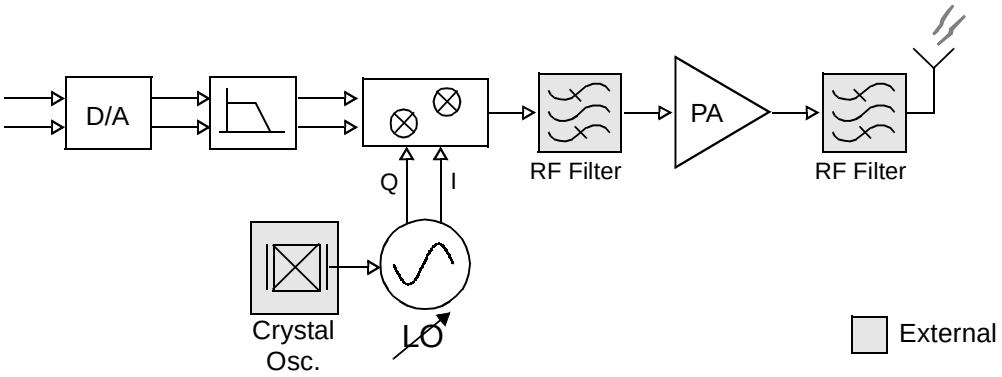

Fig. 2.7: Direct Conversion Transmitter Block Diagram.

tally modulated signal is the input to the Digital-to-Analog Converter (DAC), and the analog representation of the input signal is filtered to eliminate aliasing due to the discrete time DAC. The filtered analog waveform is up-converted directly to the carrier frequency by mixers, and it is power-amplified by the Power Amplifier (PA). External RF filters generally are required before and after the PA to eliminate noise and spurious emission in unwanted frequency bands, which limit the integrability of this architecture.

In a typical cellular telephone system, the output transmitted power can be as large as +33 *dBm*. Accounting for the insertion loss from the RF filter (worse with a duplexer), the power output from the PA may need to be 30% higher. Since the carrier frequency is identical to the LO frequency in a direct conversion transmitter, this modulated high-power PA output signal will radiate and affect the spectral purity of the nearby VCO output, which negatively impacts transmitter performance. This phenomenon is generally known as “VCO pulling” or “injection locking”.

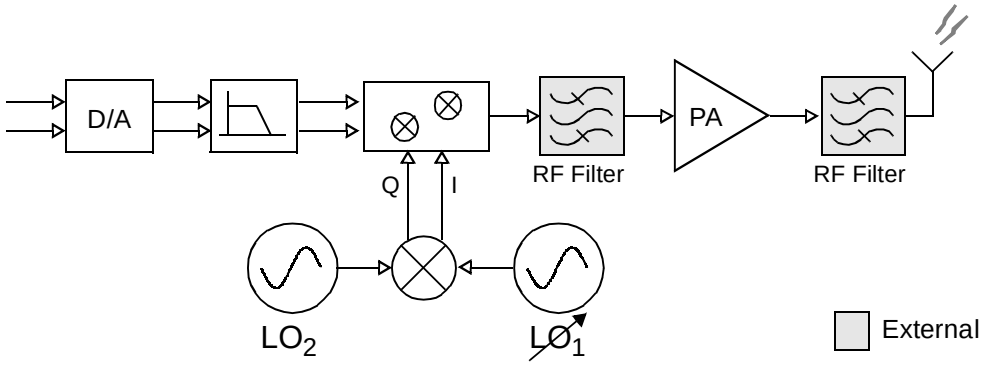

Fig. 2.8: Direct Conversion Transmitter with Offset LO.

One solution to reduce VCO-pulling problem is to use a VCO frequency different from the carrier frequency. Fig. 2.8 is a block diagram of a direct conversion transmitter using the offset LO mixing technique. The sum of the LO frequencies equals the carrier frequency; however, each LO output is not affected by the PA output because their frequencies are sufficiently far away from the carrier in the frequency spectrum. The drawback of this architecture is the generation of unwanted sideband from the offset mixing process, which may require yet an additional filter.

2.3.2 Double Conversion Transmitter

Another approach to reduce VCO-pulling is to up-convert the baseband signal in two or more steps to RF, so that the VCO frequency is far from the PA output spectrum. Fig. 2.9 is the block diagram for a *Double Conversion* transmitter. In this architecture, the baseband I/Q channels undergo the quadrature modulation at a lower frequency (LO_2),

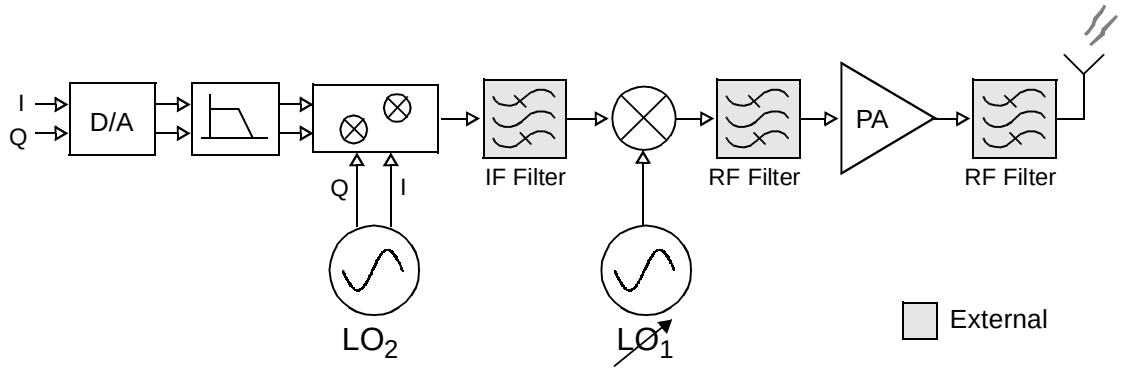

Fig. 2.9: Double Conversion Transmitter.

and the resulted IF (intermediate frequency) signal is up-converted to the transmit frequency with LO_1. The sum of the LO frequencies is the exact carrier frequency.

In addition to eliminating VCO-pulling, another advantage of double conversion over direct conversion is that the I/Q matching is better because the quadrature modulation is performed at a much lower frequency, LO_2. However, spurious tones generated by LO_2 will mix with the baseband signal to the vicinity of IF, and generating an undesired image after double conversion. This is required to be attenuated to a sufficiently low level before PA with an external filter.

In order to eliminate the external filter after LO_1 mixing, multiple phases of LO_2 can be used to generate an approximate sine wave representation of LO_2, which can minimize the harmonic mixing for low-order harmonics [29]. Furthermore, the RF filter before PA can be removed at the expense of an additional mixer stage to perform the active image rejection. Similar to frequency synthesizer considerations in the receive path, LO_2 is chosen to be variable-frequency and LO_1 to be fixed-frequency to improve the phase noise

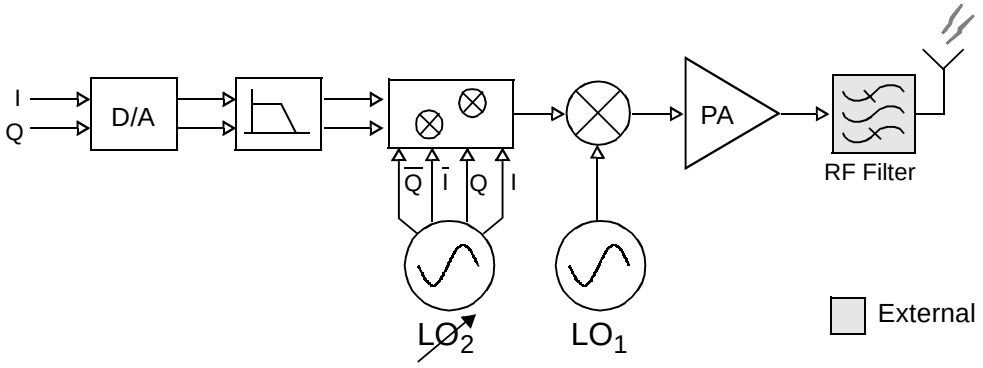

Fig. 2.10: Integrated Double Quadrature Transmitter Architecture.

performance. This architecture enables the full integration of the transmit path including the PA and is currently under investigation (Fig. 2.10) [28].

2.3.3 PLL-based Transmitter

One other approach to reduce the post-PA filtering requirement is to use a *PLL-based* transmitter architecture. This is shown in Fig. 2.11. In the conventional direct or two-step transmitter architectures, a RF filter or duplexer is required to suppress spurious emissions and transmit noise fallen in the receive band caused by up-conversion mixers [19]. However, a RF filter or duplexer is generally expensive and has a high insertion loss. The extra power required to overcome the RF filter insertion loss is very significant at this output power level and PA power-added efficiency (PAE). In [30], assuming a 50% PAE for a transmit output power of 2W, an extra 0.5-dB insertion loss from RF filter would require an additional current consumption of 136mA to compensate. This current consumption is large enough to power the entire transceiver.

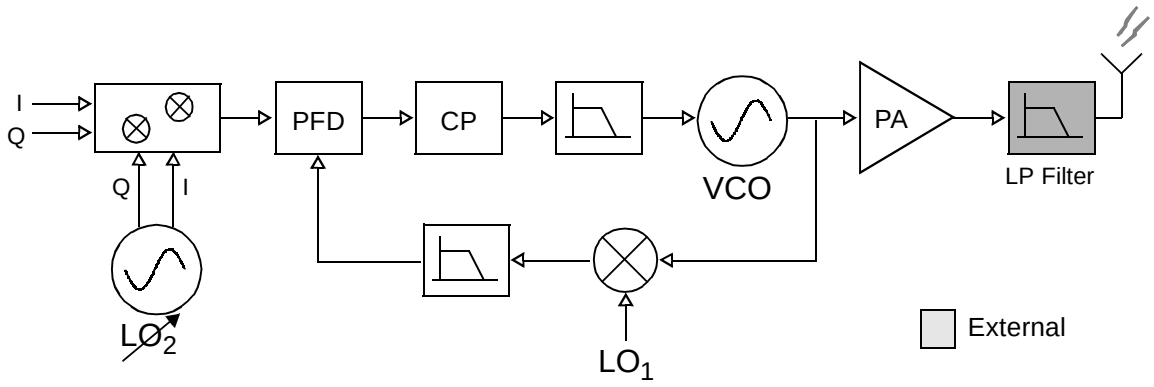

Fig. 2.11: PLL-based Transmitter Architecture.

The PLL-based transmit architecture uses a quadrature mixer to modulate the I/Q channels to IF and a frequency translation loop, instead of a second mixer, to modulate the signal to the transmit frequency. The frequency translation loop functions as a PLL where the phase/frequency detector (PFD) detects the phase difference between the IF signal and down-converted output waveform. The error signal is fed through charge pump (CP) and loop filter (LF) to generate the VCO control voltage. This architecture minimizes the spurious tone generation (i.e., the image tone) by using a PLL, and the post-PA filtering requirement is relaxed. Therefore, it allows the use of a simple low pass filter with a small insertion loss and substantially reduces the power consumption and cost of the transmitter at the expense of the circuit complexity.

2.3.4 Summary

In this section, various architectures for radio receivers and transmitters have been discussed with their operations, relative merits and integrability. Considering all aspects of each architecture with complete integration as the final goal, the wide-band IF double con-

version receiver (Fig. 2.5) and the double conversion transmitter (Fig. 2.10) are the most promising candidates. In addition to eliminating discrete high-Q filters in these architectures, they also allow new explorations of low-noise LO design techniques to synthesize a *fixed* RF frequency. This LO can potentially be integrated onto the same low-cost CMOS substrate with the rest of the transceiver. More details will be discussed in Chapter 3.

2.4 Non-idealities in Frequency Synthesizer and Their Impacts

Although there are many different types of receiver and transmitter architectures as described in earlier sections of this chapter, the frequency synthesizer function remains unchanged, namely to provide a reference frequency for the frequency translation process. In this section, a brief introduction will be given on the role of a frequency synthesizer in a receiver. Following that, the two major non-idealities of a frequency synthesizer: *phase noise* and *spurious tone*, will be presented. Their impacts on general receiver and transmitter architectures will also be discussed. More on this topic can be found in [31][32].

2.4.1 Role of Frequency Synthesizer

The role of a frequency synthesizer is to provide a reference frequency for the frequency translation function. Fig. 2.12 shows the RF section of a conventional superheterodyne architecture. The received RF signal is amplified by a LNA and filtered by the IR filter. The resulting signal is the input to the mixer. For simplicity, assuming the received signal, $f_{RF}(t)$, is a pure sine wave described by

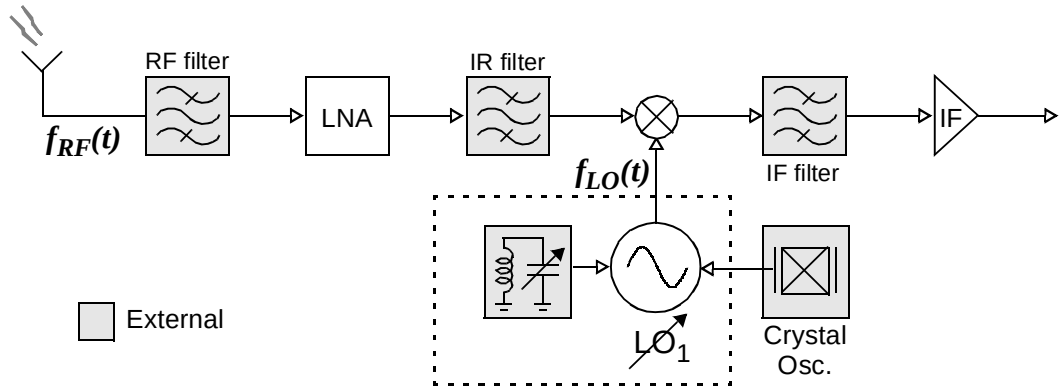

Fig. 2.12: RF Section of Superheterodyne Receiver.

$$f_{RF}(t) = a(t) \cdot \cos(2\pi f_c t + \phi) \tag{2 - 1}$$

where *a(t)* is the amplitude variation in $f_{RF}(t)$ and f_c is the desired signal frequency. An ideal reference frequency generated by the frequency synthesizer, $f_{LO}(t)$, is

$$f_{LO}(t) = b(t) \cdot \sin(2\pi f_o t + \psi) \tag{2 - 2}$$

where *b(t)* is the amplitude variation in $f_{LO}(t)$ and f_o is the LO frequency. When $f_{RF}(t)$ is mixed with $f_{LO}(t)$, the resulting waveform can be described in a mathematical formula as

$$f_{IF}(t) = f_{RF}(t) \cdot f_{LO}(t) = [a(t) \cdot \cos(2\pi f_c t + \phi)] \cdot [b(t) \cdot \sin(2\pi f_o t + \psi)] \tag{2 - 3a}$$

$$= \frac{1}{2} \cdot a(t) \cdot b(t) \cdot [\sin(2\pi(f_c + f_o)t + \phi + \psi) - \sin(2\pi(f_c - f_o)t + \phi - \psi)] \tag{2 - 3b}$$

In the case of a receiver, the up-converted term $(f_c + f_o)$ is cancelled or filtered out, and the down-converted term appears at IF where $f_{IF} = |f_c - f_o|$. Assuming the amplitude variation can be ignored, the resulting signal, $f_{IF}(t)$, is the received signal, $f_{RF}(t)$, mixed with an ideal reference frequency, $f_{LO}(t)$; it is *frequency-translated* to an IF frequency. In

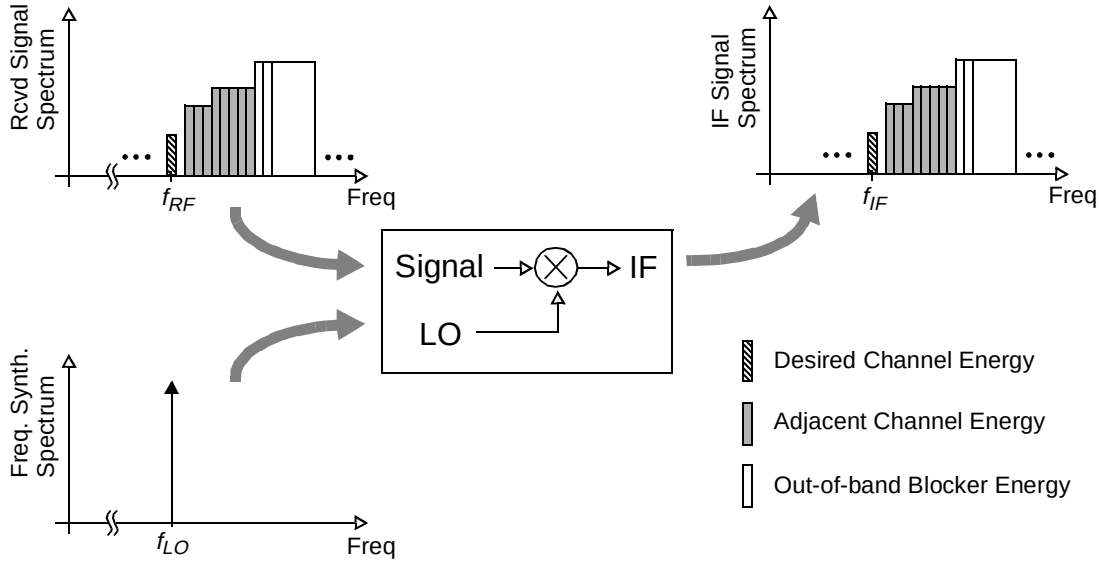

Fig. 2.13: Frequency Translation with Ideal Frequency Synthesizer Spectrum.

the case of a transmitter, the up-converted term $(f_c + f_o)$ is preserved and the down-converted term $(f_c - f_o)$ is filtered out to produce an up-converting frequency translation. Therefore, the role of a frequency synthesizer is to provide the reference frequency, $f_{LO}(t)$, for the frequency translation function.

Fig. 2.13 shows the spectral representation of the frequency translation operation for a more general case where the received signal spectrum consists of a weak desired signal and many strong adjacent channels. This case is very common in wireless communication systems today where the desired-channel user is close to the basestation while adjacent-channel users are far away. If the frequency synthesizer output is ideally a pure tone, the mixer down-converts the received signal spectrum in its entirety to an IF frequency. The respective signal strengths between desired and adjacent channels remain unchanged

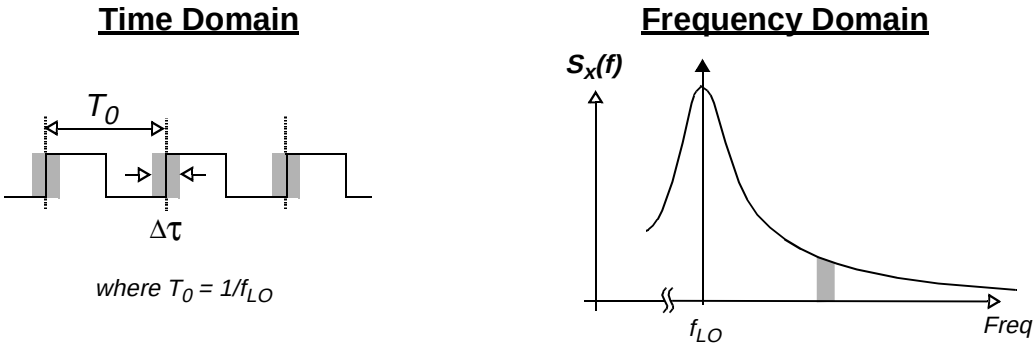

Fig. 2.14: Time and Frequency Representations of Phase Noise.

until the signal passes through the discrete IF filter. In the case of superheterodyne architecture, the discrete IF filter attenuates the adjacent channel energy significantly (Fig. 2.12).

In a real world implementation, due to system noise and mismatch, the frequency synthesizer output contains *phase noise* and *spurious tones* which are the two critical performance parameters. These will be the topics of discussion in the next two sections.

2.4.2 Phase Noise

In frequency synthesizer applications today, active circuits are often used to satisfy system requirements and to sustain oscillations in a lossy LC-tank oscillator. The random electronic noise associated with these active circuits causes uncertainties in the synthesizer output, and part of the uncertainties is considered *phase noise*.

Phase noise can be defined as the *random timing fluctuation in an oscillator period*. Shown in Fig. 2.14 (square wave is shown for simplicity) are the time and frequency

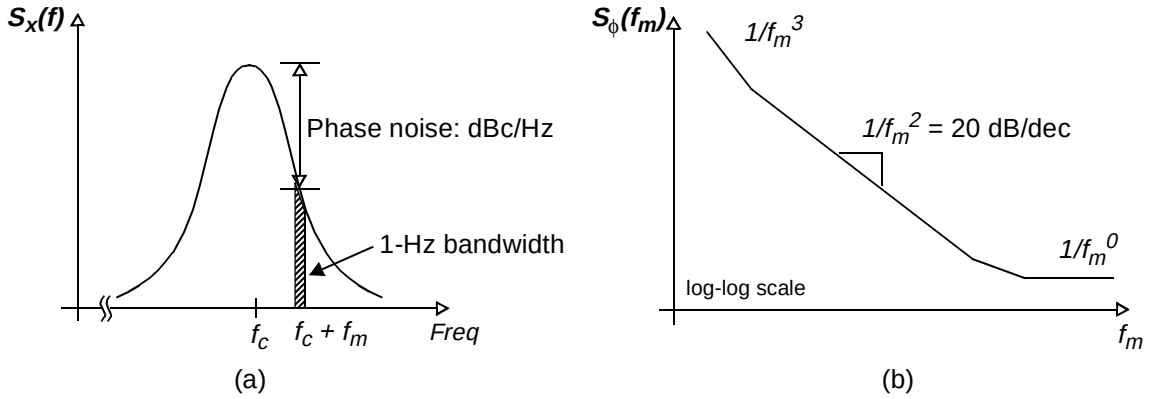

Fig. 2.15: Spectral Representations of Phase Noise.

domain representations of phase noise. In the time domain, the presence of random timing fluctuations in an oscillation period represents a low frequency noise modulated up to a RF frequency by the carrier frequency. In the frequency domain, phase noise is the noise energy around the center carrier. Ideally, an oscillator output spectrum centers at a single frequency. With the presence of phase noise, it spreads the carrier power over neighboring frequencies and creates the phase noise "skirt".

Phase noise is generally specified in *dBc/Hz* at a given offset frequency for a particular carrier. Therefore, phase noise can be found by measuring the ratio of the power spectral density (1-*Hz* bandwidth) at a given offset frequency to the total power at the carrier frequency. Fig. 2.15 shows a typical spectrum of a synthesizer output and a phase noise plot. The spectrum in Fig. 2.15(a) is the power spectrum of a synthesizer output with phase noise. The phase noise can also be drawn as in Fig. 2.15(b). In this log-log plot, phase noise (normalized to *dBc/Hz*) is plotted against the offset frequency, f_m, from the carrier, f_c. In a typical oscillator, the phase noise profile follows the curve shown, where it

traverses through $1/f_m^{\ 3}$, $1/f_m^{\ 2}$ and $1/f_m^{\ 0}$ slope regions. The $1/f^2$ region is generally referred as the "white frequency" variation region, since it is caused by white or uncorrelated timing fluctuations in the period of an oscillation. The behavior in this region is dominated by the thermal noise in the devices of the oscillator circuit. The $1/f$ flicker noise of devices also plays an important role for low offset frequencies; therefore, the spectrum in this region falls as $1/f^3$. The following subsection discusses the impact of phase noise on radio transceivers.

Receiver

A high performance superheterodyne receiver (shown in Fig. 2.12) serves as a good example to illustrate the effect of phase noise in a radio receiver. In Fig. 2.13, the frequency translation from RF to IF for a superheterodyne receiver has been shown with an ideal frequency synthesizer output. In Fig. 2.16, the ideal LO output has been replaced with a typical one having phase noise shown in the shaded areas under the curve.

In this example, the received signal spectrum consists of a weak desired channel and many strong adjacent channels. While the LO center frequency down-converts the desired channel to IF, the LO sideband phase noise energy (shown in shaded grey areas) also down-converts the adjacent channels in the received signal spectrum to IF. Since the frequency difference is the same in both cases, the down-converted adjacent channel falls in the same frequency band as the desired channel and degrades the selectivity performance of the receiver. In order to quantify the required phase noise for a typical system, an exist-

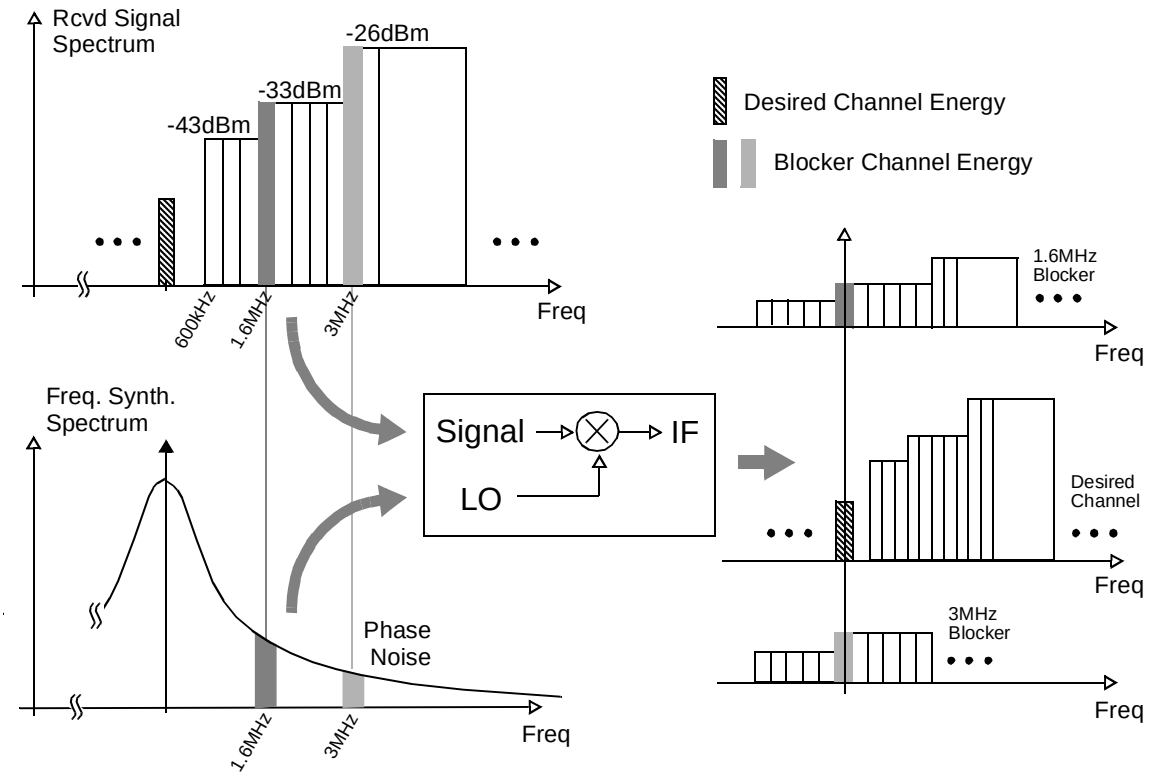

Fig. 2.16: Effect of Phase Noise in Wireless Receiver.

ing commercial wireless communication system is used as an example to calculate the phase noise requirement.

Also included in Fig. 2.16 is the blocking profile for a GSM family cellular telephone standard (DCS1800). With the reference sensitivity at -99 *dBm*, the nearest blocker is located at 600 *kHz* away from the desired channel with the maximum power of -43 *dBm*. Two stronger blockers, -33 *dBm* and -26 *dBm*, are located at 1.6 *MHz* and 3 *MHz* away from the desired channel respectively. The channel bandwidth for GSM is 200 *kHz*. To calculate the required phase noise, a few more parameters about the GSM standard must be given.

System Noise Floor = -174dBm + 10log(200kHz) = -121dBm
Reference Sensitivity = -99dBm
System Noise Figure = 7dB *(assumed)*
SNR (Signal-to-Noise Ratio) = 15dB
Output Noise Floor = -114dBm

In the GSM standard, the blocker performance is measured by first increasing the desired channel energy by 3dB from reference sensitivity or, -96dBm; as a result, the effective SNR is increased to 18dB. Then a blocker signal is applied to the receiver and increased in signal strength until the output SNR drops by 3dB; or equivalently, the blocker down-converted by the phase noise increases the overall noise by a factor of 2.

Therefore, to calculate the required phase noise, the blocker down-converted by phase noise should result in the same level as the output noise floor of the system. At 600kHz, the phase noise needs to be -124dBc/Hz; for 1.6MHz and 3MHz, the phase noise is required to be -134dBc/Hz and -141dBc/Hz respectively.

Transmitter

The function of a frequency synthesizer in a transmitter is very similar to that of a receiver shown in Fig. 2.13. It still provides a reference frequency for the frequency translation function; however, the mixer up-converts to a higher frequency.

Fig. 2.17 shows a functional block diagram of a conventional direct conversion transmitter. The digital input signal is generally a bandlimited signal that is confined within the channel bandwidth of a given system. After the D/A conversion, the LPF rejects the higher frequency aliases, and a well-conditioned baseband signal is applied to

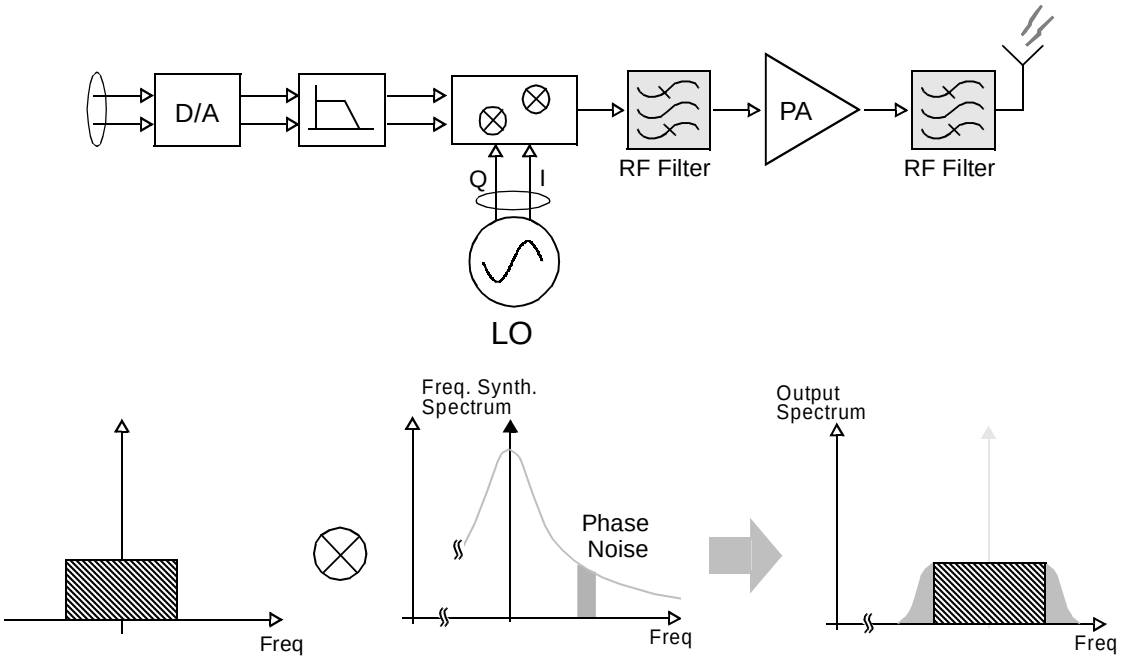

Fig. 2.17: Phase Noise Effect for Direct Conversion Transmitter.

the mixer. With an ideal frequency synthesizer output, the baseband signal is frequency translated to the RF carrier with the direct conversion transmitter.

This frequency translation process can also be easily understood with Signals and Systems theory [33]. When two signals multiply in the time domain, it is equivalent to a convolution in the frequency domain. In an ideal case, if a bandlimited signal is convolved with a single carrier tone in the frequency spectrum, the result is a bandlimited signal at the carrier frequency. This is shown with solid lines in Fig. 2.17. When phase noise is present as in a typical LO output, the convolution will “smear” the bandlimited signal by a small amount. The resulting signal will be the bandlimited signal modulated to the carrier

frequency with spectral components beyond the band edges, shown in shaded gray color in Fig. 2.17. This creates interference to neighboring channels.

To minimize the interference to adjacent channels in the system, a *spectral mask* is generally specified by the wireless standard which regulates the maximum emission power over different frequency bands allowed by a transmitter. When the phase noise is not low enough, the signal energy spilled over to adjacent channels can exceed the emission limit after the power amplification. The transmitted spectrum then fails to satisfy the emission spectral mask in the GSM family standards or the Adjacent Channel Power Ratio (ACPR) requirement in CDMA.

2.4.3 Spurious Tones

The other critical performance parameter in a frequency synthesizer is the spurious tone level. Spurious tones are normally caused by phase/frequency detector and divider circuits in the feedback control path.

Spurious tones can be defined as *systematic timing fluctuations in an oscillator waveform*. Fig. 2.18 (a square wave is again shown for simplicity) is the time and frequency domain representations of a spurious tone. In the time domain, the presence of systematic timing fluctuations in an oscillation waveform represents a periodic timing error. In the frequency domain, it manifests as the undesired tones in the frequency spectrum. Ideally, an oscillator output spectrum centers at a single frequency with no spurious tones.

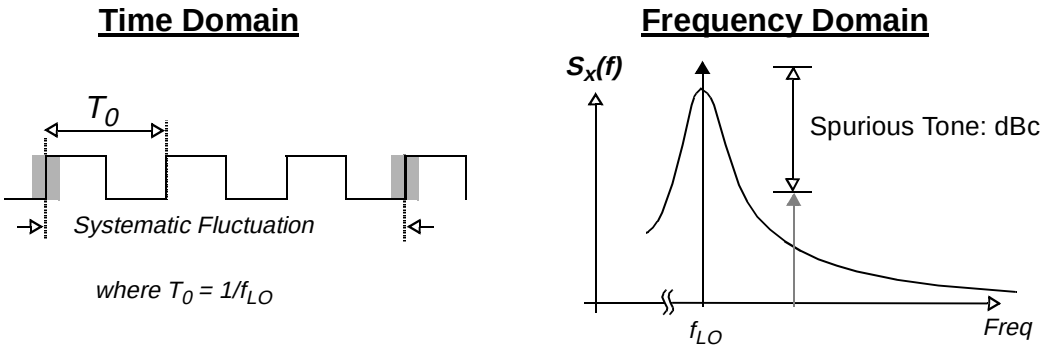

Fig. 2.18: Time and Frequency Representations of Spurious Tones.

In reality, the presence of spurious tones causes other frequency components to appear in the oscillator output spectrum.

Spurious tones are measured in *dBc* (or *dB* referenced to the carrier) at a specific frequency location in the spectrum. It is simply the power difference between the carrier and spurious tone signals in *dB*. In general, multiple spurious tones can be found in the output spectrum; and the location and magnitude of the spurious tones are related to the system design of the frequency synthesizer. The following subsection discusses the impact of spurious tones in radio transceivers.

Receiver

The effect of spurious tones in a radio receiver is very similar to that of phase noise. Fig. 2.19 shows a graphical illustration of the spurious tone effect on a superheterodyne receiver architecture. In the LO spectrum, two spurious tones are added at *1.6MHz* and *3MHz* away from the center frequency.

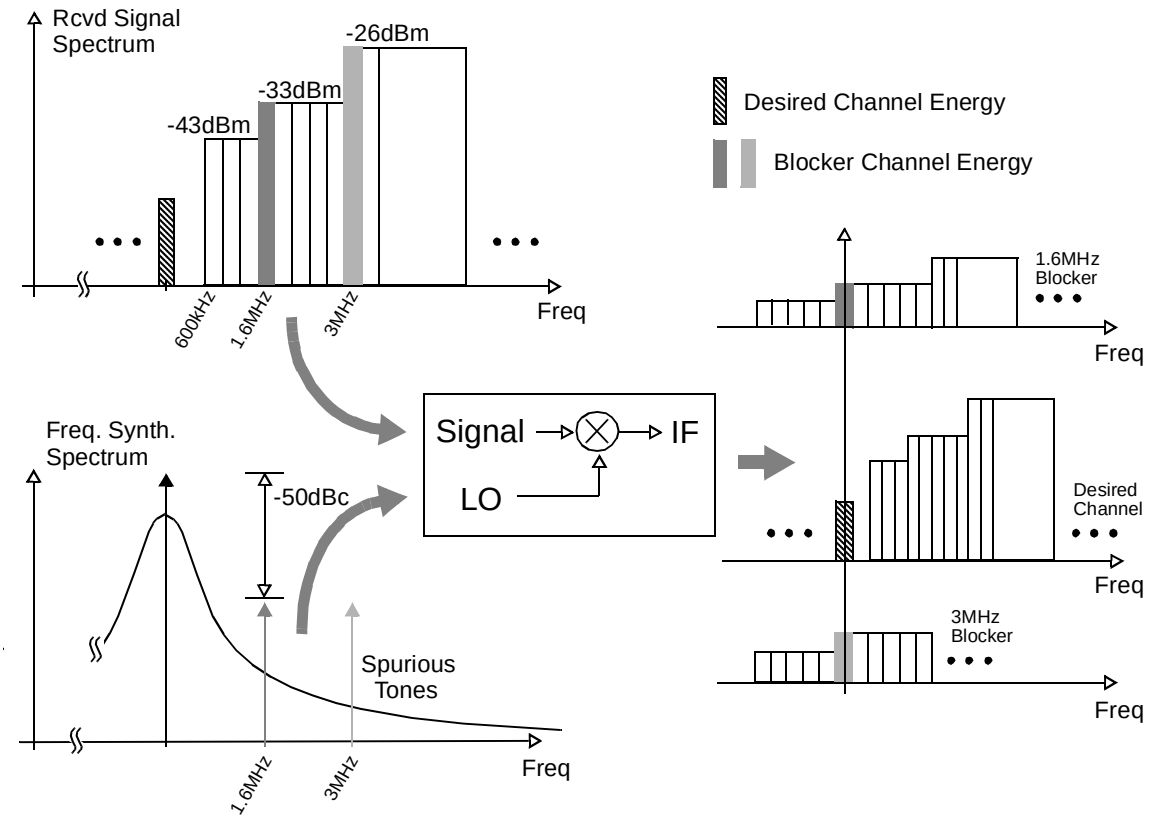

Fig. 2.19: Effect of Spurious Tones in Wireless Receiver.

In this example, the received signal spectrum consists of a weak desired channel and many strong adjacent channels. While the LO center frequency down-converts the desired channel to IF, the spurious tones in the LO output spectrum also down-convert the adjacent channels to the same IF frequency band (shown in shaded grey areas) and degrade the overall sensitivity of the receiver. However, since the spurious tones generally appear in predictable frequency locations, in most cases, a careful system design can be used to minimize this degradation.

In the GSM family standards, six inband and twelve out-of-band spurious tones are allowed with a maximum of three adjacent channel frequencies to be assigned as spurious response exceptions. In other words, a total of eighteen spurious tones can be present in the output spectrum while no more than three are consecutive channels. When a spurious response frequency is selected, the blocking requirement is relaxed to -49 *dBm* at the frequency which the blocker is applied. For the example used in the previous section (reference sensitivity is -99 *dBm*), the spurious tones need to be -50 *dBc* in order to satisfy the blocking specification.

Transmitter

Spurious tones affect the transmitter in a very similar way as the phase noise does. While the phase noise “smears” the signal bandwidth over a wider spectrum, spurious tones mixes the desired channel to RF at the spurious tone location. Fig. 2.20 is a functional block diagram of a direct conversion transmitter with its spectrum graphs to illustrate this effect.

As mentioned earlier, to minimize the interference to adjacent channels, the output spectrum of the transmitter has to follow the spectral mask provided by the wireless standard. With the presence of spurious tones due to the nature of a synthesizer architecture, some standards allow a number of exceptions to ease the radio system design. For instance, in the GSM family standards, three spurious tones are allowed within 12 *MHz* around the carrier frequency. The output power limit is -36 *dBm* in a 200 *kHz* channel in

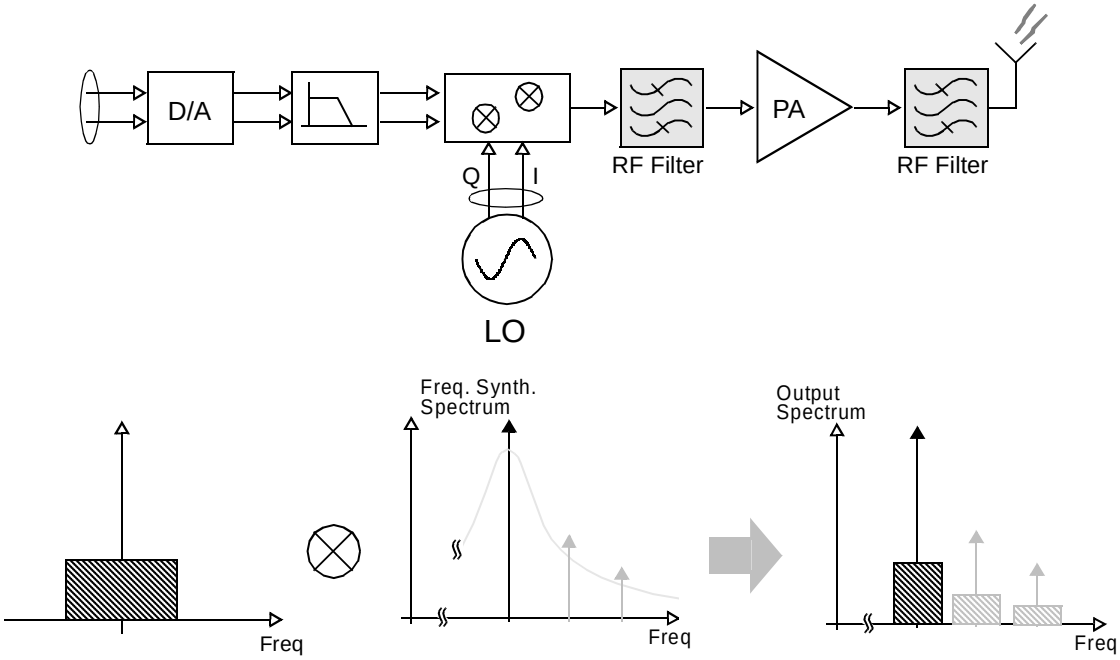

Fig. 2.20: Spurious Tone Effect for Direction Conversion Transmitter.

the transmitter. Twelve more spurious tones are allowed for frequencies beyond 6 *MHz* from the carrier with the same maximum output power of -36 *dBm.*

A more difficult specification (particularly in the GSM family standards) is the mobile station emission in the receive band. Because the mobile station receiver is very delicate, this specification is made to protect the mobile receiver sensitivity. In this specification, when the mobile station transmitter is in an active mode, the maximum power emitted from the transmitter in the receive band of the mobile station shall not exceed -71 *dBm*. The detailed calculation of the spurious tones varies among different radio and synthesizer designs.

2.5 Summary

In this chapter, a review of receiver and transmitter architectures is presented with emphasis on integrability. More detailed analysis can be found in many recently published references. The most promising architecture for the integrated receiver is the Wide-Band IF with Double Conversion architecture [26][27][28]. This architecture allows the use of a *fixed* frequency LO_1 whose benefit in terms of phase noise will be shown in the next chapter. The non-idealities of a frequency synthesizer are introduced, and their effects on radio receivers and transmitters are described. Examples of commercial applications are used to illustrate their characteristics and target performance.

In the next chapter, an introduction to the conventional design of a frequency synthesizers will be presented. It is followed by a survey of recently published integrated solutions and a comparison of their performance. The discussion of Chapter 3 will lead to the introduction of a novel approach for a local oscillator design which addresses some issues presented earlier.

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Chapter 3

Frequency Synthesizer Architectures

3.1 Introduction

Many different frequency synthesizer architectures exist for the wireless systems today; most are implemented using some form of the commonly used Phase-Locked Loop (PLL). In addition to their use in wireless communication, PLLs are also employed a variety of other functions in communication applications, such as data recovery, carrier recovery and phase modulation/demodulation.

Fig. 3.1 is a photograph of a modern digital cellular telephone Printed Circuit Board (PCB). The digital section of the system is located on the right-hand side and consists of baseband, DSP, memory, microcontroller, etc. The integration in this section is generally quite high, with a transistor count of over 100,000. The transceiver section is on the left half of the PCB, where the integration level is low, with a transistor count on the order of 100's. The transceiver uses the conventional superheterodyne architecture (discussed in

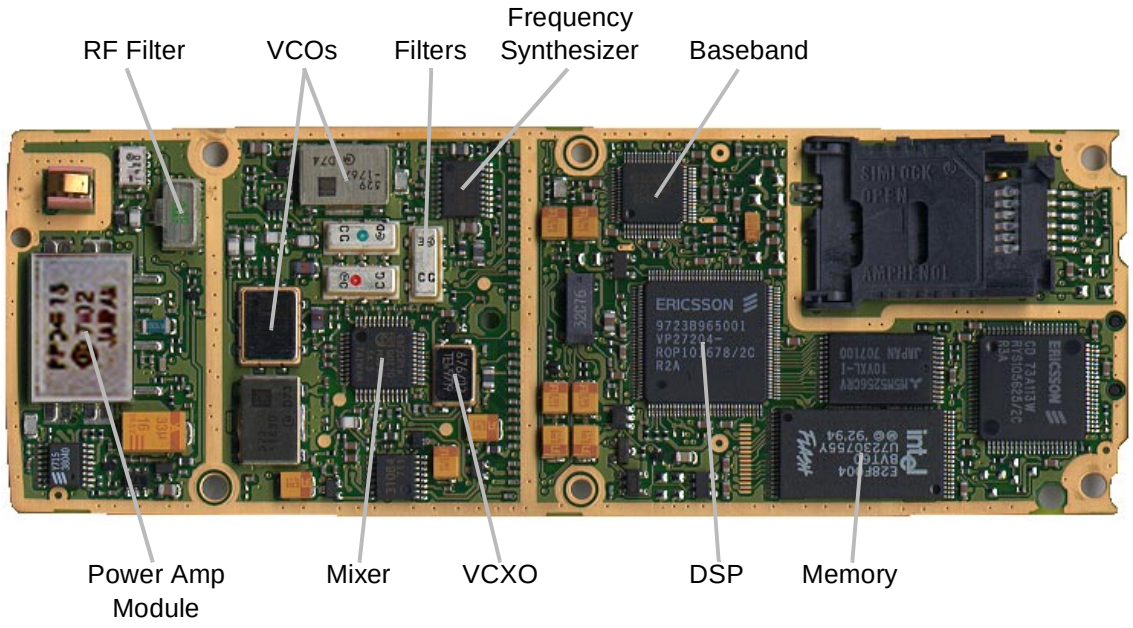

Fig. 3.1: Photograph of Ericsson 788 PCB.

Chapter 2), which is apparent from the presence of multiple discrete filters. The LO generation section has the frequency synthesizer and several large external VCOs that are used in PLLs to generate the required LO frequencies. For the monolithic transceiver design described in Chapter 1, all the RF functions need to be implemented in CMOS, so that the RF and baseband sections can be combined in a single chip. This also dictates a CMOS implementation of the frequency synthesizer and VCO functions with requisite phase noise performance as its discrete counterpart, generally a difficult task using conventional approaches.

This chapter begins with an introduction to Phase-Locked Loops, including discussion of system operation, and its impact on the output *phase noise* and *spurious tones*. A brief discussion of a current commercial PLL implementation which utilizes a discrete

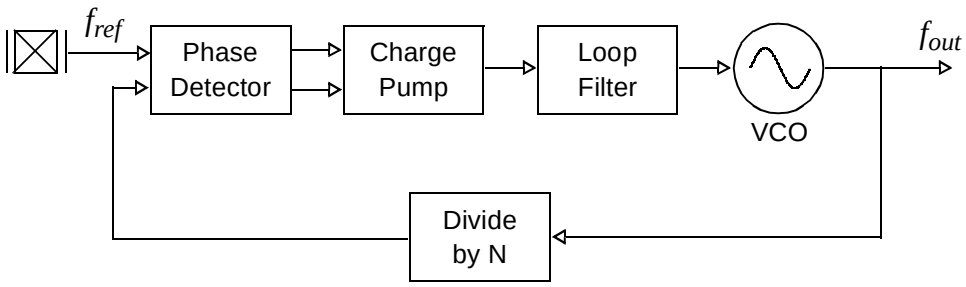

Fig. 3.2: Simplified Block Diagram for Phase-Locked Loop.

LC-tank VCO to achieve low phase noise performance is included. This approach is similar to the LO solution used in the Fig. 3.1 example. A survey of recently published integrated VCOs for wireless communication systems is presented to show the trend toward higher integration. Several integrated VCOs use available on-chip active/passive devices and explore the process and packaging technology. Although these integrated VCOs have the same characteristics as a discrete implementation, their phase noise performance is inadequate for modern wireless communication systems (i.e., GSM, AMPS, TDMA, etc.). A discussion of common characteristics and performance limitations of integrated VCOs is presented in the next section, followed by a novel approach that addresses the performance limitations of the current integrated VCO design.

3.2 Phase Locked Loop Fundamentals

Fig. 3.2 is a simplified block diagram of a Phase-Locked Loop (PLL). The components of a PLL generally include a phase detector, charge pump, loop filter, divider and Voltage-Controlled Oscillator (VCO). The basic functionality is as follows. The output

frequency from the divider is first compared to the reference frequency by the phase detector. A phase error signal generated by the phase detector is passed to the charge pump and creates a signal whose magnitude is proportional to the phase error. This signal is then low-pass filtered by the loop filter and used to control the output frequency with the VCO. When the PLL is in the locked condition, the two inputs to the phase detector are *in-phase* (or a *fixed* phase offset), and the output frequency is equal to the reference frequency multiplied by the divider ratio, *N*.

This section gives a brief description of the PLL linearized model. The performance limitation in terms of phase noise and spurious tone is discussed, followed by an existing commercial example used in a cellular telephone application.

3.2.1 PLL Linearized Model

There are many variations of PLLs available on the market today since each of the components in the PLL can be designed in different ways. Digital implementations of PLLs can also be found for some specific applications [36]. Despite these PLL derivatives, understanding the fundamentals is still a good starting point. As the name suggests, PLL locks the phase of the VCO output to the reference signal phase. During the initial transient, PLL goes into nonlinear operating region as the VCO tries to find the correct frequency. As soon as the loop is in the locked condition, the small-signal linearized model can be used.

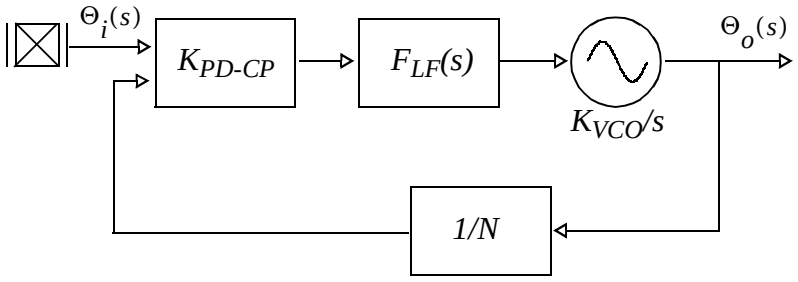

Fig. 3.3: Small-Signal AC Model of PLL.

Fig. 3.3 is a small-signal AC model of each building block in the PLL. The phase detector compares the phase difference between two inputs, and the charge pump converts the phase difference into a voltage signal. K_{PD-CP} denotes the composite phase detector and charge pump transfer function in units of $volts/radian$. The charge pump output is filtered by the lowpass filter and generates a control voltage for the VCO. The transfer function for the loop filter is $F_{LF}(s)$, and the filter output varies the output frequency of the VCO. Because phase is the integral of frequency, the *S-domain* transfer function for VCO is K_{VCO}/s. The divider in the feedback path divides the VCO output frequency by *N* and has a transfer function of $1/N$.

In the steady state, the *s-domain* phase transfer function from input to output is

$$\frac{\Phi_o(s)}{\Phi_i(s)} = \frac{G(s)}{1+G(s)} = \frac{K_{PD-CP}\cdot F_{LF}(s)\cdot K_{VCO}/s\cdot 1/N}{1+K_{PD-CP}\cdot F_{LF}(s)\cdot K_{VCO}/s\cdot 1/N}. \qquad (3\text{-}1)$$

If $F_{LF}(s)$ is constant, the transfer function is a first order system which is unconditionally stable. In a typical implementation, a pole/zero pair is used in $F_{LF}(s)$ to increase the frequency range and flexibility of the PLL. For example, if $F_{LF}(s)$ is

$$F_{LF}(s) = K_{LF} \cdot \frac{s+z}{s+p}, \tag{3 - 2}$$

the transfer function becomes second-order:

$$\frac{\Phi_o(s)}{\Phi_i(s)} = \frac{Ks + Kz}{s^2 + (K+p) \cdot s + Kz}, \tag{3 - 3}$$

where

$$K = (K_{PD-CP} \cdot K_{LF} \cdot K_{VCO})/N. \tag{3 - 4}$$

A practical loop filter design has a pole at the origin and a zero before the PLL loop bandwidth. In the example above, if $p = 0$,

$$\frac{\Phi_o(s)}{\Phi_i(s)} = \frac{(K_{PD-CP} \cdot K_{LF} \cdot K_{VCO})/N \cdot (s+z)}{s^2 + (K_{PD-CP} \cdot K_{LF} \cdot K_{VCO})/N \cdot s + (K_{PD-CP} \cdot K_{LF} \cdot K_{VCO})/N \cdot z}. \tag{3 - 5}$$

At high frequency, $|F(j\omega)| = K_{LF}$, and $|G(j\omega)| = 1$ when $\omega = (K_{PD-CP} \cdot K_{LF} \cdot K_{VCO})/N$. Therefore, the PLL bandwidth is

$$\omega_{-3dB} = (K_{PD-CP} \cdot K_{LF} \cdot K_{VCO})/N. \tag{3 - 6}$$

Eq. 3 - 5 is the phase transfer function and it can be used to derive transfer functions from any given point in the PLL system to the output. For example, Fig. 3.4 shows possible noise sources associated with the functional blocks in the small-signal AC model. Noise sources associated with phase detector and charge pump, $V_{n1}(s)$, and divider,

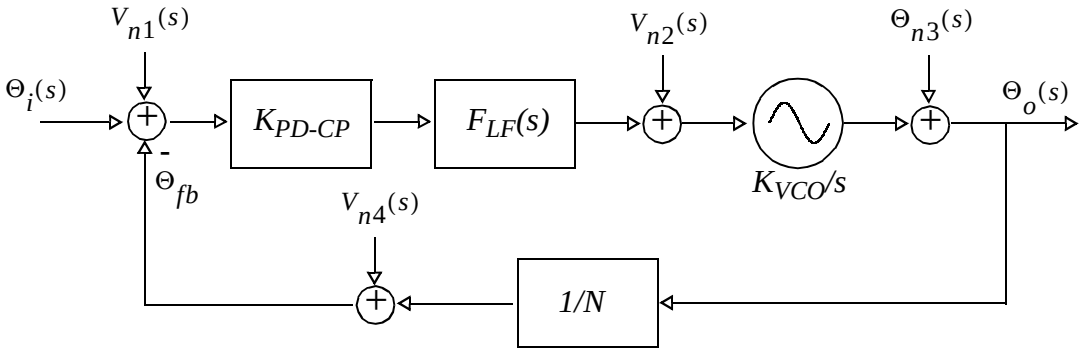

Fig. 3.4: Small-Signal AC Model of PLL with Noise Sources.

$V_{n4}(s)$, appear at the feedback summation. These noise sources experience the PLL transfer function (Eq. 3 - 5) enhanced by the divider ratio *N*.

$$H_1(s) = \frac{\Phi_o(s)}{V_{n4}(s)} = \frac{1}{1+G(s)} \cdot N = \frac{(K_{PD-CP} \cdot K_{LF} \cdot K_{VCO}) \cdot (s+z)}{s^2 + (K_{PD-CP} \cdot K_{LF} \cdot K_{VCO})/N \cdot (s+z)}. \quad (3\text{ - }7)$$

The loop response to the noise injected at the output of the loop filter, $V_{n2}(s)$, is

$$H_2(s) = \frac{\Phi_o(s)}{V_{n2}(s)} = \frac{1}{1+G(s)} \cdot \frac{K_{VCO}}{s} = \frac{s \cdot K_{VCO}}{s^2 + \frac{(K_{PD-CP} \cdot K_{LF} \cdot K_{VCO})}{N} \cdot (s+z)}. \quad (3\text{ - }8)$$

The phase noise present in the VCO, $\Phi_{n3}(s)$, is shaped by

$$H_3(s) = \frac{\Phi_o(s)}{\Phi_{n3}(s)} = \frac{1}{1+G(s)} = \frac{s^2}{s^2 + (K_{PD-CP} \cdot K_{LF} \cdot K_{VCO})/N \cdot (s+z)}. \quad (3\text{ - }9)$$

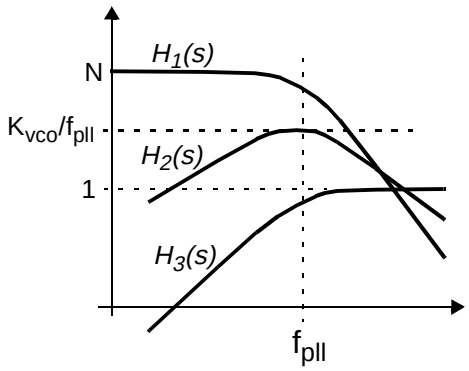

Fig. 3.5: Transfer Functions for Eq. 3 - 7, Eq. 3 - 8, and Eq. 3 - 9.

Using above transfer functions (also shown in graphical form in Fig. 3.5), one can attempt to understand the performance limitation of PLLs in the next section. For more in-depth PLL analysis and its variations, see [37] and [38].

3.2.2 Performance Limitation

One of the major phase noise contributors in PLL is the VCO phase noise. In order for a PLL to synthesize small channel spacings directly (i.e., 200 *kHz* in GSM family standards), the reference frequency needs to be equal to or multiple of the channel spacing. For stability and validity of the small-signal AC model, the PLL loop bandwidth needs to be much smaller than the comparison frequency, in general ten times smaller. With a loop bandwidth in the tens of kHz, the high-pass transfer function from the VCO to output (Eq. 3 - 9) only rejects the phase noise in the frequency band below the PLL loop bandwidth and passes all the higher-frequency phase noise to the output. In a conventional design, the VCO is generally implemented with discrete varactors and inductors (or modules shown in Fig. 3.1); its phase noise performance is very good. Therefore, even with a small loop

bandwidth, the phase noise performance can still be satisfactory. As shown in the next section that integrated VCOs tend to have a higher phase noise due to the low quality factor of the spiral inductor. Hence, a higher suppression of phase noise from the PLL transfer function in a monolithic implementation is required in order to satisfy the phase noise requirements of cellular systems.

Fig. 3.5 shows that other noise sources experience different transfer functions to the output. For the noise present at the phase detector input, the transfer function is a low-pass filter. The noise is enhanced by the divider ratio in the passband and falls off beyond the PLL loop bandwidth. For the noise at the charge pump output, it is subject to a bandpass response where the passband of the bandpass transfer function depends on the pole/zero location of the loop filter. Due to practical constraints, conventional designs set the PLL bandwidth at a very low frequency, so the effect of the noises mentioned above is negligible. However, if the PLL bandwidth is increased in order to obtain a higher suppression for the VCO phase noise, more noise is passed to the output from other sources. A careful examination of each noise source is then necessary.

3.2.3 Current Approach

One of the most popular frequency synthesizers today for RF personal communications is LMX2332L by National Semiconductor [39]. Fig. 3.6 is a functional block diagram of the IC. LMX2332L is a dual frequency synthesizer with both RF and IF inputs and two charge pump outputs. The RF/IF inputs pass through the prescalers and counters,

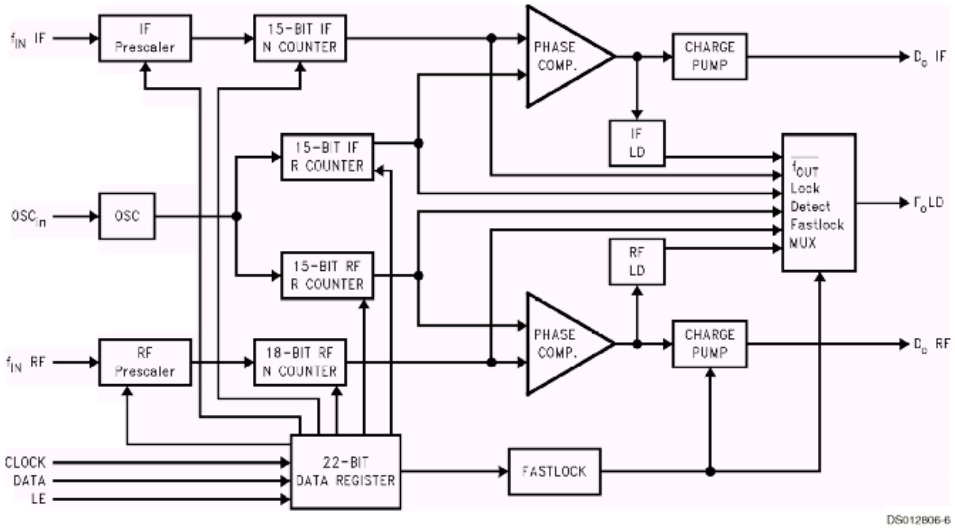

Fig. 3.6: Functional Block Diagram of National Semiconductor LMX2332L.

then are compared with the phase of the oscillator input (OSC_{in}). The phase comparison result is used as the UP/DN pulse in the charge pump. The charge pump outputs are filtered by the off-chip loop filters and used to control the frequencies of the external VCOs which provide the RF/IF inputs.

Fig. 3.7 shows a typical application. The discrete components include the loop filters, VCOs and bypass capacitors. The typical values of loop filter capacitors and resistors are shown in Fig. 3.7, and they set the loop bandwidth of approximately 20kHz. Using a discrete VCO, the single sideband phase noise is measured at -72.6dB at 150Hz away from the carrier frequency and satisfies the AMPS specifications. (This standard will be described in more detail in Chapter 6). LMX2332L is fabricated in a 0.5μm BiCMOS process and nominally consumes 3.0mA from a 3.3V supply.

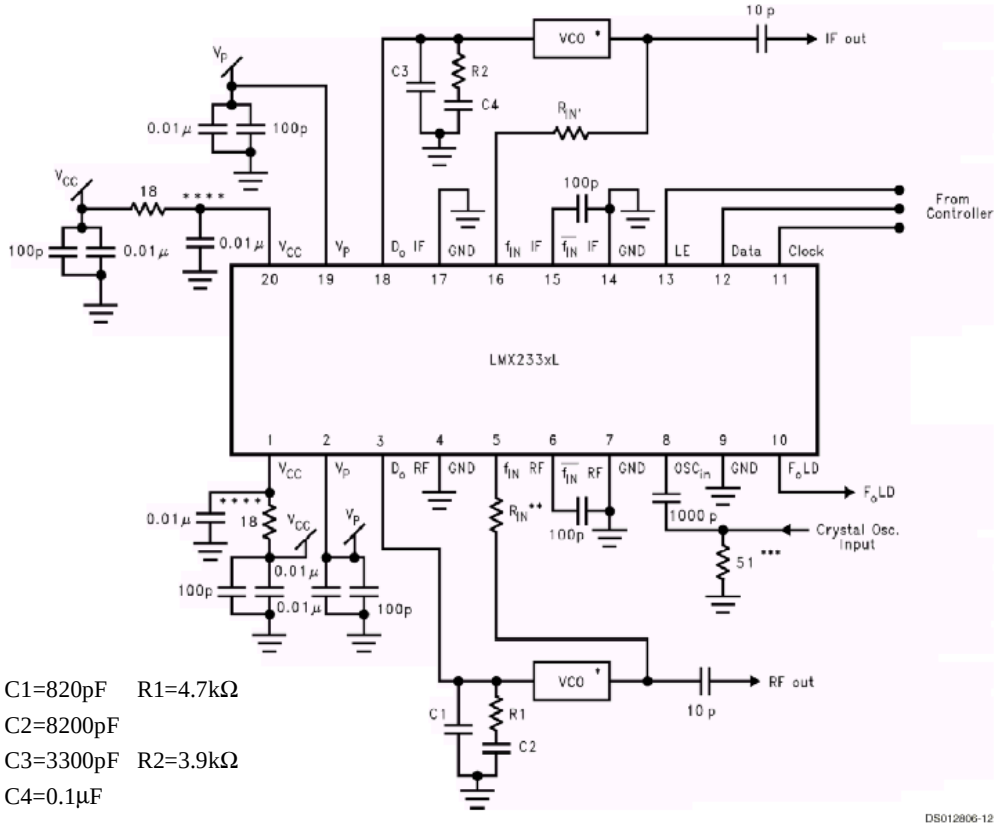

Fig. 3.7: Typical Application of National Semiconductor LMX2332L.

3.3 Integrated Voltage Controlled Oscillators

To make a single-chip radio, the discrete LC-tank components currently used in commercial implementations need to be integrated onto the silicon substrate without degrading overall LO performance. There are many challenges for the integration of LC-tank components. Although capacitors are standard components in CMOS technology, varactors with a large tuning range need to be designed by using different doping profile regions in the CMOS process while maintaining a high quality factor. Furthermore, induc-

tors are non-standard components in CMOS process; several attempts have been made to create inductors suitable for wireless application in the CMOS technology.

The most widely used integrated inductor on a silicon substrate is the planar spiral inductor, which can be easily implemented with the available metal layers in any standard process [40]. Research has also been done on post-processing or micromachining steps to improve the quality of integrated inductors. Since the ultimate goal is to integrate the entire PLL function on the same substrate with the RF and baseband sections, methods of implementing VCOs without integrated inductors have also been explored. This section surveys recent publications on integrated VCOs for wireless applications. The survey is divided into four sections according to the difference in inductor structures. They are *Monolithic Integrated LC-tank with Spiral Inductors, Process Enhanced Inductors, Inductor-less Ring Oscillator VCOs* and *Micromachined-base VCOs*. The pros and cons of each VCO are discussed individually, and their references are provided for further studies.

3.3.1 Monolithic Integrated LC-tank

The most straightforward way to integrate a LC-tank VCO onto the CMOS substrate is to make on-chip inductors from spiral metal layers and p+/n-well varactors. Two representative examples using this method are summarized below. Examples with spiral inductors designed in different technologies can be found in recent publications. The first example below reported the best phase noise performance to date for an integrated LC-tank, and the second example has been successfully integrated into a commercial product.

Optimized Hollow Spiral Inductors

As mentioned earlier, the noise performance of a frequency synthesizer largely depends on the noise performance of its VCO. In a conventional VCO design with LC-tank, the phase noise performance, $L(\omega)$, is inversely proportional to the quality factor of the LC-tank, as shown in this equation,

$$L(\omega) \propto \frac{1}{P_s} \cdot \left[1 + \left(\frac{\omega_o}{2Q\omega}\right)^2\right], \qquad (3 - 10)$$

where Q is the quality factor of the LC-tank and ω_o is the output frequency in radians. In the monolithic implementation, the series resistance associated with the p+/n-well on-chip varactor can be minimized with a careful design and layout. Therefore, the Q for the LC-tank is generally limited by the quality factor of the *inductor*. The quality factors for varactors and inductors are

$$Q_{varactor} = \omega RC, \quad Q_{inductor} = \frac{\omega L}{R}. \qquad (3 - 11)$$

In [41], a VCO was implemented using planar spiral inductors and p+/n-well varactors in a standard 0.7μm two-metal CMOS process. The inductors are octagonal and designed with a hollow center. The Q of the inductor was estimated to be 5.7, and the phase noise was measured to be -116 *dBc/Hz* at 600 *kHz* offset from a carrier frequency of 1.88 *GHz*.

Integrated VCO in a Digital Cordless Telephone

Most of the integrated VCOs in publications today are still in the research-and-development phase. One example [42] has been implemented successfully into a commercial product for a spread spectrum digital cordless telephone. The chip contains the entire PLL with on-chip loop filter and VCO. The LC oscillator is implemented with square spiral inductors and p+/n-well varactors; the varactors are complemented with a binary-weighted capacitor array to increase the tuning range. The phase noise was measured to be -105 *dBc/Hz* at 200 *kHz* offset from a carrier frequency of 1.6 *GHz*. This chip is implemented in a 0.6μm triple-metal CMOS process.

A similar PLL is integrated with a single-chip CMOS direct-conversion transceiver for a 900 *MHz* spread spectrum digital cordless telephone [43]. Although the phase noise of this integrated PLL is higher than that of a discrete implementation, the less restrictive blocker specification of the digital cordless telephone than cellular standards allows the use of integrated PLLs to provide the LO signals.

3.3.2 Process-Enhanced Inductors

It has been shown in the last sections (Eq. 3 - 10) that the performance of a VCO largely depends on the quality of the inductor used in the LC-tank. Several attempts have been made to use additional processing steps that are compatible with the CMOS process to enhance the quality factor and self-resonance frequency. These are normally done after the standard CMOS process, i.e., the removal of silicon substrate and the use of bond-wires.

LC-Oscillator with Quadrature Outputs using Suspended Inductor

In addition to the resistive loss in the substrate (which is the main factor for the lower inductor Q factor, given in Eq. 3 - 11), the other major problem for the integrated planar spiral inductor with a large inductance is self-resonance. In a typical CMOS process, metal layers used for planar spiral inductors are only a few μm from the silicon substrate. For a high inductance planar spiral inductor, large area and multiple turns are required; as a result, the parasitic capacitance of the metal layers can be large. For example, inductors as large as 10 *nH* on a standard silicon substrate self-resonate at 2 *GHz* [40]. For the validity of the inductor model and consideration of process variations, an accurate spiral inductor design requires the operating frequency to be much lower than the self-resonance frequency. Therefore, this limits the attractiveness of high-value spiral inductors in a standard CMOS process.

In a typical CMOS process, although the thickness of the silicon wafer is 500μm, the MOS devices are constructed on the top surface with no more than a few μm of diffusion penetration into the substrate. The main reason for having a thick wafer is to increase the mechanical strength for handling during processing. Removing the substrate after the process is complete has no effect on the active devices. Therefore, if the substrate underneath the planar spiral inductor can be removed in post-processing, the parasitic capacitance and resistive loss in the substrate can be reduced. In [44], a 100-*nH* inductor was designed with the selective EDP wet etch [45] to remove the substrate under the inductor. The self-resonance frequency of the inductor increased from 800 *MHz* to 3 *GHz*. This inductor

has been used in several wireless applications [46]. Although this inductor enjoys a high self-resonance frequency and lower substrate resistive loss, the extra post-processing steps required, processing yield and reliability are still being carefully studied.

One of the examples using the substrate-etched suspended inductor mentioned in the previous section is in [47]. In a modern wireless system, quadrature oscillator outputs are required to perform image rejection and other functions in the mixer. The conventional LC-oscillator design provides a single output; an I/Q generator is then required to produce the quadrature signals. By cross-connecting two LC-oscillators as in [47], quadrature outputs appear at the two outputs of the LC-oscillators. The Q factor for this large inductor is found to be approximately 5 at 1 *GHz*, and the phase noise achieved is -85 *dBc/Hz* at 100 *kHz* offset.

Bondwire Inductors

Bondwires have been the standard connection method between integrated circuits and the outside world for decades. The parasitic inductance associated with bondwires has been a source of problems in IC technology, especially for high speed and high frequency IC. However, one can use bondwires (made of aluminum or gold) to create a high quality on-chip inductor. In [48], a 1.8 *GHz* VCO was implemented in a 0.7μm CMOS technology. Two pairs of bondwires were used to create the inductance required for the LC-tank. The parasitic inductance of bondwires is approximately 1 *nH* per *mm*; therefore, a reasonable bondwire length can be used for 1-2 *GHz* applications. The parasitic capacitance for this structure with bondwires is dominated by the bonding pads compared with spiral

inductors, where all the metal strips contribute. Hence, the self-resonance frequency is quite high.

In [48], the single-sideband phase noise was -115 *dBc/Hz* at 200 *kHz* offset from a 1.76 *GHz* carrier. The result indicated improvements in the noise performance over planar spiral inductors due to the higher quality factor of bondwire inductors. However, the inductance control and IC packaging present challenges for this design. Due to several uncertainties in the bonding process, e.g., height, distance, straightness of the bondwires, the actual inductance value will vary from the designed value. Since each wire is individually bonded, the matching between a pair of bondwires is poor. Furthermore, the suspended bondwire between two bond pads on the same die (or two separate dice) makes the plastic injection package impractical.

3.3.3 Integrated Ring Oscillator VCO

Another approach to implement the integrated VCOs is to use ring oscillators, which do not require on-chip inductors. Different output frequencies are achieved by adjusting the time delay of each element in the ring oscillator, and the oscillator's noise depends on the thermal noise contribution of each active device in the circuit. Implementations of ring oscillators can be categorized into two types according to switching behavior, *fixed swing* and *full switching.*

Fixed Swing Ring Oscillator VCO

One way to implement a ring oscillator VCO is to use source-coupled logic with NMOS differential input devices and PMOS triode-region load devices. The benefits of

using a fully differential ring oscillator are its good power supply rejection and process variation immunity. The output voltage swing is fixed by using a replica bias circuit to control the resistance of the PMOS triode region load devices. The phase noise of the ring oscillator is predicted by deriving the thermal-noise-induced *r.m.s.* timing error for each individual delay stage and extending that for the positive-feedback ring oscillator. The measured phase noise result fit well with the analysis, and the phase noise vs. power consumption trade-off from the analysis also agrees with the experimental data.

More information about the ring oscillator design can be found in [49]. A similar source-coupled logic circuit is used in the experimental prototype of this thesis and details are shown in Chapter 6.

Full Switching Ring Oscillator VCO

Another way to implement a ring oscillator VCO is to allow full switching of devices in the delay stage. When the delay stages are turned completely on or off, no thermal noise is present at the output; however, when the delay stage is during transition, thermal noise appears in the transitional edge. This noise is difficult to analyze due to the nonlinear characteristic of the ring oscillator feedback system; it can only be approximated by the switching operations on the thermal noise current during transitions. In order to minimize the thermal noise contribution for this approach, delay stages in the ring oscillator must have fast switching transitions.

The maximum frequency achievable by a ring oscillator is limited by the minimum time delay through a delay stage. Because the time delay of a delay stage largely depends on the weaker PMOS device, the dual-delay scheme is used in [50] to minimize the time delay per delay stage. This scheme includes both the negative skewed and normal delay paths. While the normal delay path is connected to the NMOS device of the CMOS inverter, the negative skewed delay path is connected to the PMOS to provide the weaker device an early transition signal. The VCO using this approach was fabricated in a 0.6μm CMOS technology with a measured phase noise of -101 *dBc/Hz* at 100 *kHz* and -117 *dBc/Hz* at 600 *kHz* for a 900 *MHz* carrier frequency.

3.3.4 Micromachined-Based VCO

One other method to create high-Q LC-tank on CMOS substrate is to use micromachined inductors and capacitors. It involves non-standard CMOS process, and therefore, will not be discussed in this dissertation. However, references are provided for more information [51][52][53][54].

3.3.5 Summary

The survey in this chapter indicates that many attempts have been made to integrate VCOs onto silicon substrate. Because the phase noise performance of a PLL largely depends on the Q factor of the LC-tank, the limiting factor in the integrated approach is the poor planar spiral inductor Q. Although the phase noise performance with spiral inductors is suitable for cordless telephone applications with a careful PLL design [43], it is still

insufficient for cellular applications with integrated transceiver architectures. Post-processing and micromachining steps give new possibilities in improving the inductor Q and self-resonance frequency; however, these additional processing steps are costly and may decrease the processing yield. Although the ring oscillator VCO does not require integrated spiral inductors, the thermal noise contribution from each delay stage is accumulated in the oscillating cycle and creates a relatively high phase noise for low offset frequencies. This noise accumulation is also true for other oscillators, and their phase noise curve is shaped by the LC-tank. Other recent publications on integrated VCO are in the reference [55][56][57][58][59][60][61][62][63].

3.4 Architecture Alternatives for Frequency Synthesizers

In the conventional receiver design (See “Superheterodyne” on page 11), the channel-select LO_1 needs to synthesize small frequency steps at RF. As a result, the loop bandwidth of the PLL is required to be much smaller than the reference frequency or channel spacing. Although this loop transfer function with a small loop bandwidth does not attenuate the VCO phase noise, by using discrete VCOs with high-Q components, meeting the requirements of a cellular application is not very difficult [39].

When a higher integration is desired, VCOs must be integrated on-chip. Shown in the last section, the monolithic VCOs generally have a poor phase noise performance due to the poor inductor Q factor. By using the conventional receiver architecture where a small loop bandwidth PLL is required for LO_1, it does not provide any suppression for the

poor integrated VCO phase noise. Furthermore, the capacitor values in the loop filter are often very large and not cost-effective to integrate.

3.4.1 Wide Loop Bandwidth PLL

In the GSM standards (a popular Personal Communication Systems - PCS), the channel spacing is 200 *kHz*, and the nearest blocker is located at 600 *kHz* away from the desired channel. To reduce the phase noise of integrated VCOs to a level that satisfies this standard, a wide loop bandwidth of PLL can be used to suppress the phase noise inside the loop bandwidth frequency (described in Eq. 3 - 9). Fig. 2.5 is the proposed integrated receiver architecture. This architecture, with a *fixed-frequency* LO_1, allows the PLL to have a high loop bandwidth to suppress the close-in phase noise of integrated VCOs. *Channel selection* is then performed with LO_2 where the operating frequency is much lower, and the phase noise is inherently better. Recent works [50] and [64] have demonstrated this technique using a wide loop bandwidth PLL where the low offset frequency phase noise is reduced.

The side effect of a wide loop bandwidth is that it opens up the PLL bandwidth and allows other noise sources in the PLL to contribute to the output phase noise. The noise transfer functions from the phase detector and loop filter to the PLL output are lowpass and bandpass respectively (described in Eq. 3 - 7 and Eq. 3 - 8). By having a wider loop bandwidth, these transfer functions allow additional noise to pass through from the divider, phase detector, etc. (in some cases, the phase noise is actually enhanced by the

divider ratio, *N*). This then affects the alternate channel rejection of the receiver. Therefore, low-noise circuits need to be carefully designed in a wide bandwidth PLL.

3.4.2 New Architecture for Narrow-Channel Wireless System

For wireless systems with very narrow-channel spacings (i.e., 30 *kHz* in AMPS/ TDMA), the phase noise requirement becomes increasingly difficult. The phase noise of a VCO increases at 20 *dB/dec* (Fig. 2.15) as the offset frequency decreases (it increases at 30 *dB/dec* when including the *1/f* effect). Therefore, it is very difficult to design the PLL loop bandwidth to have sufficient attenuation to suppress the close-in phase noise of an integrated VCO for narrow-channel systems. Shown in previous sections, the main factor of poor phase noise for an integrated VCO using LC-tank is the low-Q inductor. Much of recent research has focused on enhancing the quality factor of integrated inductors by different means. However, the inductor Q and phase noise performance are still lagging in a standard CMOS process with no extra post-processing steps.

In the case of a ring oscillator VCO [50], the timing jitter associated with each inverter is accumulated from cycle to cycle. This accumulation of timing jitter causes the low-frequency phase noise to be high and results in a phase noise curve approaching infinity at an arbitrary low-offset frequency. Depending on the design, this VCO also experiences 1/f flicker noise contribution from active devices. Therefore, these sources all affect the overall performance of the VCO.

The above discussion shows that a new frequency synthesizer architecture is needed in order to satisfy the demanding requirements of a narrow-channel wireless system. The following chapters discuss a novel approach to building a monolithic frequency synthesizer. Its phase noise does not depend on the integrated spiral inductor quality factor, and its timing jitter does not accumulate from cycle to cycle. Chapter 4 will be the introduction of the new concept, followed by a detailed analysis of this particular architecture. Implementation details of the prototype are described in Chapter 5 and 6; the test setup and experimental results are in Chapter 7.

3.5 Summary

In this chapter, the fundamentals of a Phase-Locked Loop are introduced with PLL operation and system design equations. A typical commercial implementation using external VCOs was shown. A survey of integrated VCOs, which utilize several different methods to improve the quality factor, was presented. These methods include *Monolithic Integrated LC-tank with Spiral Inductors*, *Process Enhanced Inductors*, *Inductor-less Ring Oscillator VCOs* and *Micromachined-base VCOs*. Finally, the trade-offs between narrow and wide loop bandwidth in a PLL are characterized with an integrated receiver architecture example. A new frequency synthesis architecture that does not require oscillating circuits and high-Q spiral inductor for the phase-noise challenged, narrow channel spacing wireless systems will be discussed in the next chapters.

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Chapter 4

DLL-based Frequency Multiplier Fundamentals

4.1 Introduction

Chapter 3 described the most commonly-used frequency synthesizer architecture, PLL. The loop equation suggests that for a conventional PLL design with discrete VCOs, phase noise performance largely depends on the VCO phase noise due to the small loop bandwidth. Block down-conversion makes possible a fully-integrated transceiver architecture (Fig. 2.5) with a fixed-frequency LO_1 and a programmable LO_2 (as in the WBIFDC architecture). This technique allows new low-phase-noise local oscillator designs, such as a wide loop bandwidth PLL that suppresses the phase noise of an integrated VCO within the loop bandwidth [65]. However, the phase noise performance with a wide loop bandwidth PLL is still inadequate for narrow-channel wireless communication systems. This chapter introduces a novel design for a fixed-frequency local oscillator. The phase noise of this design does not depend on the integrated inductor quality factor, and the random timing error does not accumulate from cycle to cycle.

This chapter first introduces the basics of the DLL-based frequency multiplier. The approach to achieving low-phase-noise and the operation of DLL are described. This is followed by a detailed noise analysis that predicts the phase noise performance for the frequency multiplier. This chapter concludes with the implications and applications of this low-phase-noise DLL-based frequency multiplier design.

4.2 The Basics

The DLL-based frequency multiplier approach takes advantage of the inherently low jitter of a low-frequency crystal oscillator reference to produce a low-phase-noise RF signal. This is accomplished by taking each relatively jitter-free but infrequent edge of the crystal oscillator output, and from that generating a burst of well-controlled evenly spaced edges that span one period of the crystal oscillator. These evenly-spaced edges are combined to form a pattern of higher-frequency transitions and eventually generate the desired RF signal. Therefore, the phase noise in the bands of interest is closely related to that of the reference crystal. This concept is illustrated in Fig. 4.1. Unlike conventional VCO-based frequency synthesizers, thermal-noise-induced timing edge uncertainties accumulate within one period of the crystal oscillator, consequently the phase noise does not increase within the crystal frequency. Given the extremely high Q and consequently very low phase noise of crystal oscillators, the overall phase noise of the RF output signal

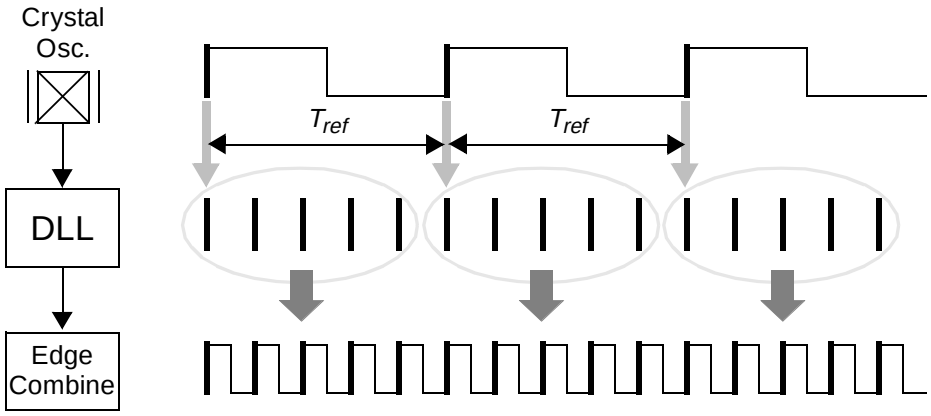

Fig. 4.1: DLL-based Frequency Multiplier Concept.

for this approach can be much lower than that of typical synthesizers using integrated VCOs.

4.2.1 Operation

To generate the well-controlled and evenly-spaced edges shown in Fig. 4.1, a delay-locked loop (DLL) with identical delay stages is needed. On the left of Fig. 4.2 is a conceptual block diagram of the DLL-based frequency multiplier. The reference crystal frequency is the input of the delay chain. Each delay element produces a delayed version of the reference crystal waveform. The phase detector senses the phase difference between the input and output of the delay chain and generates an error signal. This error signal controls a charge pump, whose output is filtered by the loop filter. The filter output is the control voltage that varies the time delay of each delay stage to minimize the phase error. When the loop is in the locked condition, the input and output of the delay chain are

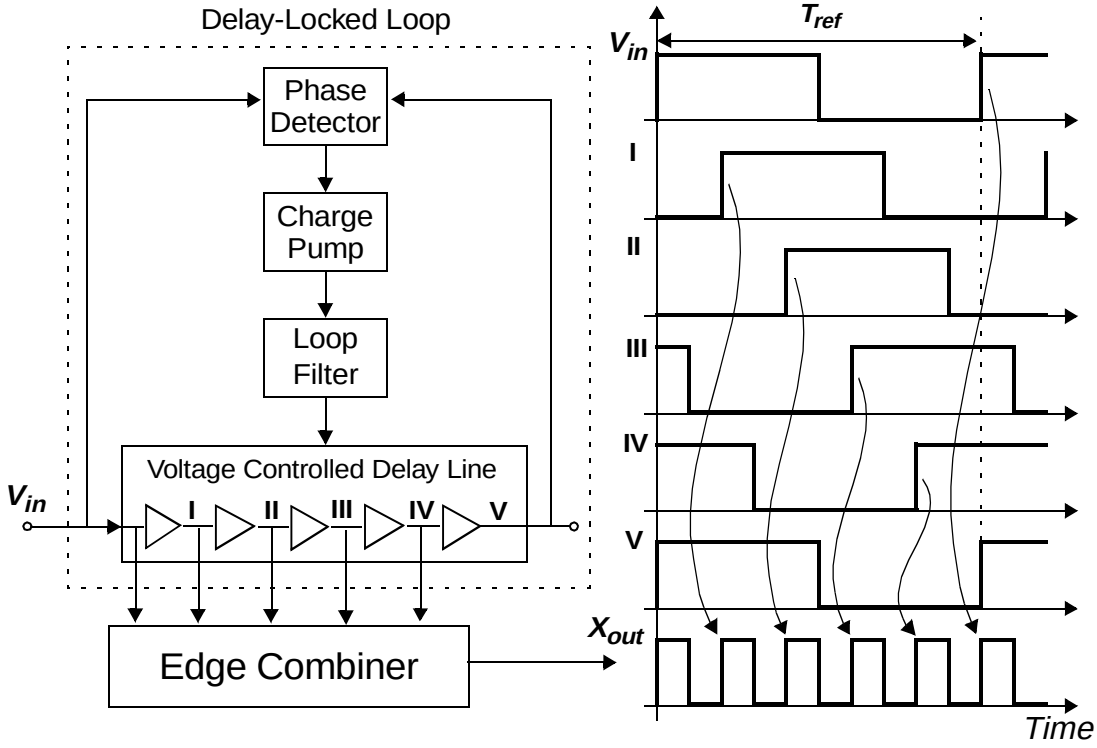

Fig. 4.2: Operation for DLL-based Frequency Multiplier.

in-phase. The outputs of delay elements generate waveforms with edges that are evenly spaced within one period of the reference crystal.

For the five-delay-stage example in Fig. 4.2, the output waveform of the first stage is delayed $\frac{1}{5} \cdot T_p$ from the crystal reference waveform, where T_p is the crystal reference period. The output waveform of the second delay stage is delayed $\frac{1}{5} \cdot T_p$ from the previous output, and so on. When the loop is in the locked condition, the output of the last delay stage is *in-phase* with the reference crystal waveform. The output of the DLL equally divides the reference period by 5, and the sum of the time delays from all delay stages is precisely one period of the reference oscillation, T_p.

To generate the RF signal, the edge combiner block produces oscillations in the local oscillator output from each rising edge in the DLL outputs (Fig. 4.2). When the end of the delay chain is reached, since the last DLL output is *in-phase* with the crystal oscillator input, the next edge to trigger the LO output is from the low-jitter crystal oscillator. Repetitions of this process generate the LO waveform. Hence, the local oscillator output for this example is 5 times the crystal reference frequency, or in a general case, N times the crystal reference frequency, where N is the number of delay stages. Another way to describe the edge combiner operation is by using a N-tap FIR model. This is described in Chapter 5.

4.2.2 Timing Jitter Accumulation

A DLL-based frequency multiplier using a voltage-controlled delay chain has an inherent advantage over a PLL using a voltage-controlled oscillator. Fig. 4.3 shows timing jitter accumulation for an oscillator compared with that of a DLL-based frequency multiplier. In an oscillator (for example, a ring oscillator shown in Fig. 4.3), random timing errors accumulate because the timing jitter at the end of each oscillation is the starting point of the next. The random timing error of the output signal is the sum of the timing errors of all previous oscillations. This translates to a poor long-term jitter performance, or, equivalently, poor close-in phase noise. Fig. 4.3 shows that the random timing uncertainty for a ring oscillator increases as a function of time.

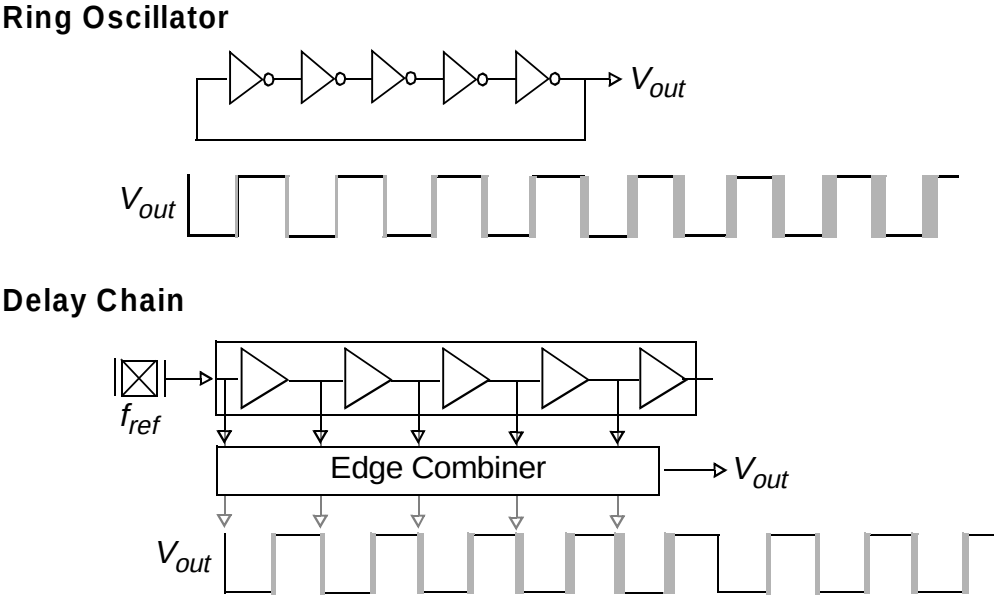

Fig. 4.3: Timing Jitter Accumulation for Ring Oscillator vs. Delay Chain.

In contrast, for a finite-length delay chain in the DLL-based frequency multiplier, the random timing error accumulates only within a single delay chain cycle. The timing error in one cycle of the delay chain does not affect the next cycle, because the waveform that triggers the next output oscillation is the reference crystal waveform. This provides *excellent long-term* jitter performance, or, equivalently, a low close-in phase noise.

The different phase noise signatures of a PLL with a voltage-controlled oscillator (VCO) and a DLL-based frequency multiplier can also be understood by examining the source of synthesized output waveform. In a PLL, the output signal is taken directly from a VCO (as shown in Fig. 3.2) whose timing uncertainties accumulate over many oscillation cycles, limited by the time response of the PLL in which it is embedded. However, the PLL bandwidth is constrained by practical considerations to a value several orders of

magnitude lower than the output frequency. In contrast, each output edge from the DLL only contains the timing uncertainties accumulated from the previous delay stages within the same crystal oscillation period (shown in Fig. 4.3). Limited jitter accumulation gives a flat phase noise profile for offset frequencies less than f_{ref}. The long-term timing error accumulation, equivalent to the close-in phase noise, is much lower than that of a typical VCO. This is extremely important for wireless systems with very narrow channel-spacings.

4.3 Performance Analysis

This section estimates analytically the phase noise characteristics and performance of the DLL-based frequency multiplier described in the previous section, then discusses spurious tones. The analysis includes results from previous published research [66][67][68] and random process theory [69][70][71][72]. A summary of each is included in Appendix A & B for completeness.

4.3.1 Phase Noise

The most important performance specification for a frequency synthesizer is the phase noise. Phase noise is the random timing fluctuation in an oscillator period. Fig. 4.4 shows a sinusoidal waveform with timing uncertainties. Assuming the random timing error of the waveform occurs at the zero crossing point and can be defined as the discrete-time random process, $X(t)$, the sinusoidal waveform can then be written as,

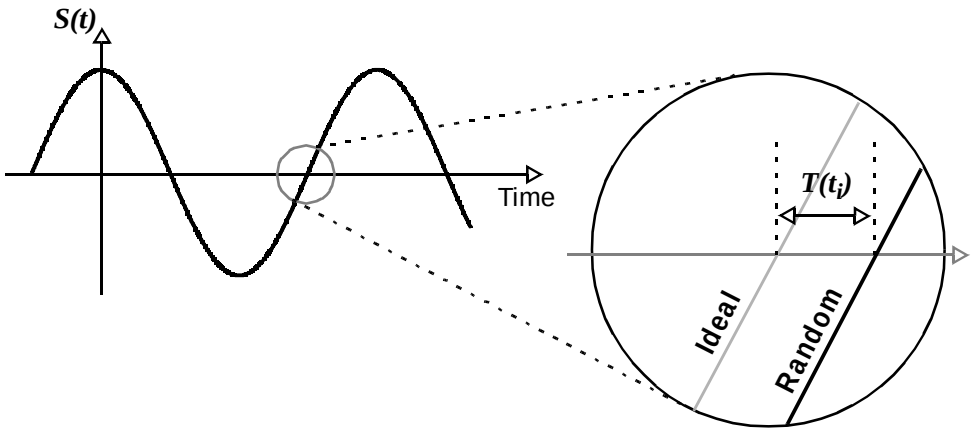

Fig. 4.4: Timing Uncertainties in a Sinusoidal Waveform.

$$S(t) = A(t) \cdot \cos\{2\pi f_c[t - X(t)]\}, \qquad (4 - 1)$$

where $A(t)$ is the amplitude, f_c is the carrier frequency in *Hz*. By applying a trigonometric identity, Eq. 4 - 1 can be re-written,

$$S(t) = A(t) \cdot \cos(2\pi f_c t) \cdot \cos[2\pi f_c X(t)] + A(t) \cdot \sin(2\pi f_c t) \cdot \sin[2\pi f_c X(t)]. \qquad (4 - 2)$$

The random timing error is generally much smaller than the oscillation period, $X(t)$ can be approximated with a discrete-time impulse function,

$$X(t) \Rightarrow X(n\bar{T}) \qquad n \in I, \qquad (4 - 3)$$

where $\bar{T}$ is the period of the carrier frequency, or $\frac{1}{f_c}$; and

$$\cos[2\pi f_c X(n\bar{T})] \cong 1, \text{ and } \sin[2\pi f_c X(n\bar{T})] \cong 2\pi f_c X(n\bar{T}), \qquad n \in I. \qquad (4 - 4)$$

Eq. 4 - 2 can then be approximated by

$$S(t) \cong A(t) \cdot \cos(2\pi f_c t) + A(t) \cdot [2\pi f_c X(n\bar{T})] \cdot \sin(2\pi f_c t), \qquad (4 - 5)$$

in which the carrier power (first term) and noise power (second term) are clearly separated into two terms. The phase noise term is a low frequency noise component modulated up to the carrier frequency by $\sin(2\pi f_c t)$.

Phase noise is typically measured as the power spectral density of the noise as a function of frequency compared to the carrier power at the carrier frequency; specified in *dBc/Hz*. In most cases, due to the circuit limiting effect, the oscillation amplitude is constant, A. Phase noise can be written as

$$\frac{Noise\ Power}{Carrier\ Power} = \frac{\frac{1}{2}(A \cdot 2\pi f_c)^2[S_{X(n\bar{T})}(f)]}{\frac{1}{2} \cdot A^2} = (2\pi f_c)^2[S_{X(n\bar{T})}(f)], \qquad (4\text{-}6)$$

where the carrier signal is a deterministic signal with power is $A^2/2$. For noise power, since $X(n\bar{T})$ is a random process, the power spectral density, $S_{T(t)}(f)$, is used to find its power. Therefore, the noise power is $(A \cdot 2\pi f_c)^2[S_{X(n\bar{T})}(f)]/2$. Eq. 4 - 6 suggests that, in order to estimate the phase noise for this waveform, the power spectral density (PSD) of the random process, $X(n\bar{T})$, needs to be estimated.

The phase noise performance of a DLL-based frequency multiplier is limited by the inherent phase noise of the crystal oscillator and the timing jitter contributed by the delay chain and edge combiner. Crystal oscillator phase noise is very important, since the jitter noise power associated with each crystal edge propagates into the delayed edges generated from it. However, due to the extremely high Q of available crystal oscillators, this source of noise is not an important contributor in the applications of interest. The following

assumes that the major contributor to the phase noise is the voltage-controlled delay chain. Other noise sources are discussed in Section 4.4 and in the circuit implementation section in Chapter 5.

Timing Jitter Accumulation

To find the power spectral density, $S_{X(n\bar{T})}(f)$, the random process $X(n\bar{T})$ can be further defined according to the jitter accumulation pattern of the DLL-based frequency multiplier. As described earlier in this chapter, the output waveform of each delay stage in the DLL-based frequency multiplier triggers an oscillation in the final output (Fig. 4.2). Assuming the edge combiner is noiseless, the random timing error associated with the output waveform of each delay stage *directly* shows up in the final output waveform as random timing error. $T(t)$ is the random process that describes the random timing error of the final output waveform due to the delay stages as a function of time.

Although the analytical equations below describe a general case, to help illustrating the analysis, a 5-stage delay chain is shown in figures (i.e., Fig. 4.5). For simplicity, the following assumptions are made. The delay chain is driven directly by a perfect crystal reference with no timing jitter. The random variable y_{ij} is the random timing error associated with a delay stage. The index i, $1 \le i \le 5$, indicates the specific delay stage. In the DLL-based frequency multiplier, the timing jitter accumulates within one cycle of the delay chain but does not affect the next cycle. Therefore, it is necessary to have the second index j which denotes the specific number of delay-chain cycles. Random variable, y_{ij}, is

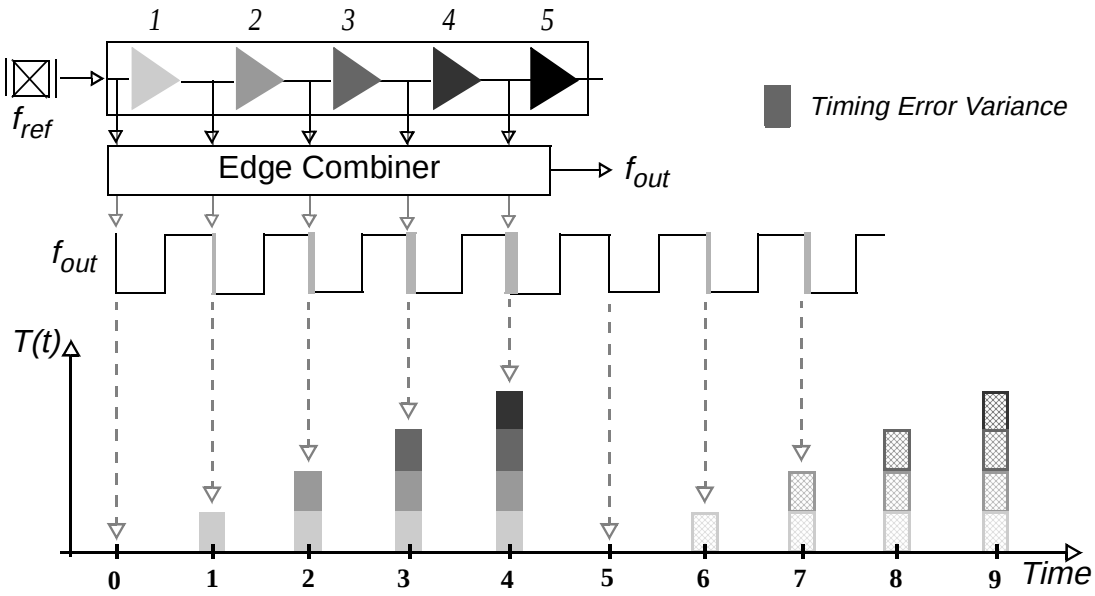

Fig. 4.5: Timing Error Accumulation for Five-Stage Delay Chain.

independent from random timing errors of other delay stages, zero mean and Gaussian distributed with variance σ^2.

$$E[y_{ij}] = 0, \quad E[y_{ij}^2] = \sigma^2. \tag{4 - 7}$$

With the above definitions and assumptions, $X(n\bar{T})$ can now be written according to the random timing error of delay stages. In Fig. 4.5, the first output oscillation is triggered by the crystal reference input. Assuming that crystal reference has no timing error, the first term $X(0) = 0$. The next output oscillation is triggered by the output of the delay *Stage 1*, hence the timing error uncertainty is associated with the delay *Stage 1*. Because this is the first pass through the delay chain, the random process $X(1 \cdot \bar{T}) = y_{11}$. The different shades of gray in Fig. 4.5 indicate the correspondence between delay stage and the random variable, y_{ij}. The next output oscillation is triggered by the output of the delay *Stage 2* and its

timing error is $X(2 \cdot \bar{T}) = y_{11} + y_{21}$, which is the sum of random timing error variables associated with delay *Stages 1* and *2*. Similarly, the timing errors for following two oscillations are found to be $X(3 \cdot \bar{T}) = y_{11} + y_{21} + y_{31}$ and $X(4 \cdot \bar{T}) = y_{11} + y_{21} + y_{31} + y_{41}$. The general expression for the random process up to this point is

$$X(n \cdot \bar{T}) = \sum_{i=1}^{n} y_{i1}, \quad \text{for } n < 5. \tag{4 - 8}$$

When the end of the delay chain is reached, the next oscillation is triggered by the next incoming crystal reference edge and hence has no timing error: $X(5 \cdot \bar{T}) = 0$. The following oscillation is again triggered by the delay *Stage 1*; however, the timing error for the second delay chain cycle is independent of that of the first cycle, therefore, $X(6 \cdot \bar{T}) = y_{12}$. In the same way, $X(7 \cdot \bar{T}) = y_{12} + y_{22}$ and so on. In Fig. 4.5, a different fill pattern is used to denote the second cycle. The general expression for $X(n\bar{T})$ is

$$X(n\bar{T}, j) = \sum_{i=1}^{n-(j-1)\cdot N} y_{ij}, \tag{4 - 9}$$

where N is the number of delay stages in the delay chain, and n is a positive integer less than N. The graph in Fig. 4.5 represents the random process of timing jitter at different points in time as a function of random timing error variable associated with each delay stage. It also captures the independence of random timing error between different delay chain cycles.

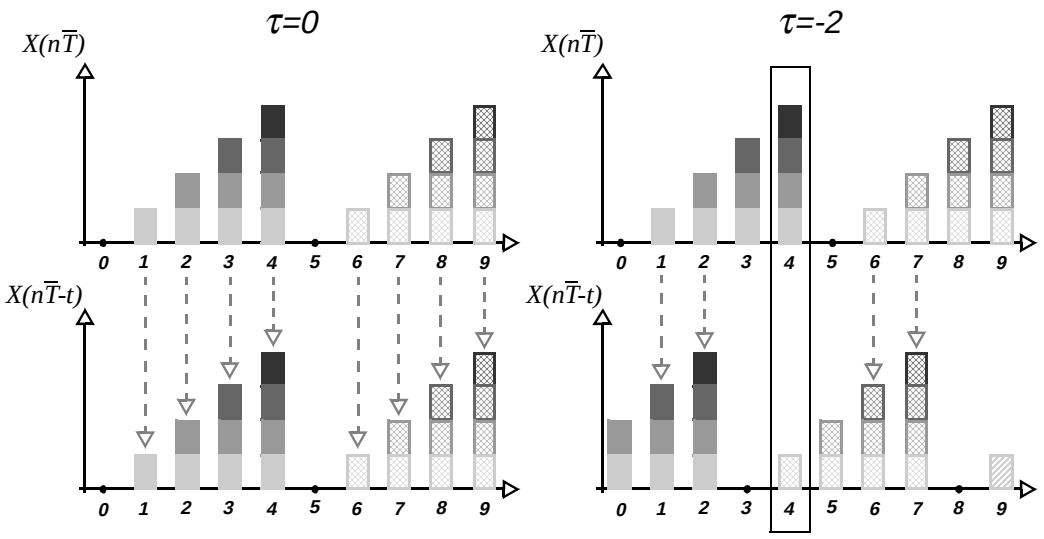

Fig. 4.6: Autocorrelation Operation of Random Process $X(n\bar{T})$.

Power Spectral Density of Timing Error Random Process

One way to find the power spectral density (PSD) of the timing error random process is to find the *Fourier Transform* of autocorrelation function

$$R_{XX}(\tau) = E[X(n\bar{T}) \cdot X(n\bar{T} - \tau)]. \qquad (4\text{ - }10)$$

When $\tau = 0$, the autocorrelation equals the variance of the random process. For $N = 5$,

$$R_{XX}(0) = E[X(n\bar{T}) \cdot X(n\bar{T})] = \frac{1}{5} \cdot (0 + \sigma^2 + 2\sigma^2 + 3\sigma^2 + 4\sigma^2) = 2 \cdot \sigma^2. \qquad (4\text{ - }11)$$

This is shown on the left side of Fig. 4.6. The factor of $1/5$ comes from the autocorrelation function (see Appendix B). When $\tau = 1$, the autocorrelation function is the expected value of the random process multiplied by a shifted version of itself and summed,

$$R_{XX}(1) = E[X(n\bar{T}) \cdot X((n-1)\bar{T})] = \frac{1}{5} \cdot (0 + \sigma^2 + 2\sigma^2 + 3\sigma^2 + 0) = 1.2 \cdot \sigma^2. \qquad (4\text{ - }12)$$

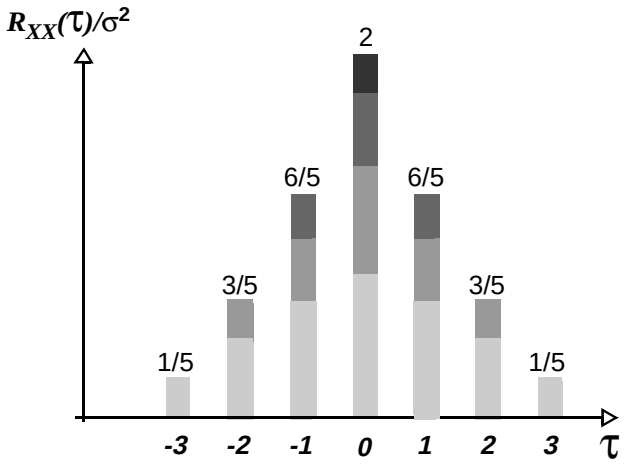

Fig. 4.7: Autocorrelation of Timing Error Random Process for Five-Delay-Stage Example.

When $\tau = 2$, the random timing errors of first cycle overlap with that of the second cycle in the shifted version (shown in the right side of Fig. 4.6). However, since the timing errors are independent from cycle to cycle, the correlation for the overlapped section (indicated in Fig. 4.6) is zero. Therefore,

$$R_{XX}(2) = E[X(n\bar{T}) \cdot X((n-2)\bar{T})] = \frac{1}{5} \cdot (0 + \sigma^2 + 2\sigma^2 + 0 + 0) = 0.6 \cdot \sigma^2. \quad (4\text{-}13)$$

The same approach gives $R_{XX}(\tau)$ other values of τ. Fig. 4.7 shows the autocorrelation function for the 5-stage example. The general expression for the autocorrelation function is

$$R_{XX}(\tau) = \frac{1}{N} \cdot \sum_{k=-(N-2)}^{N-2} \left[\delta(\tau - k) \cdot \sum_{l=1}^{N-|\tau|-1} l \cdot \sigma^2 \right], \quad (4\text{-}14)$$

where N is the number of delay stages in the delay chain.

If, previously assumed, the random timing error per stage is much smaller than the oscillation period, a Discrete-Time Fourier Transform (DTFT) can be applied to the above autocorrelation function, Eq. 4 - 14, to approximate the power spectral density (PSD). The result is

$$S_X(\Omega) = \sum_{n=-\infty}^{\infty} R_{XX}(n) \cdot e^{-j\Omega n}. \qquad (4 - 15)$$

Combining Eq. 4 - 14 and Eq. 4 - 15, the general expression for the PSD becomes

$$S_{XX}(\Omega) = \sum_{n=-\infty}^{\infty} \left\{ \frac{1}{N} \cdot \sum_{k=-(N-2)}^{N-2} \left[\delta(n-k) \cdot \sum_{l=1}^{N-|n|-1} l \cdot \sigma^2 \right] \right\} \cdot e^{-j\Omega n}, \qquad (4 - 16)$$

where σ^2 is the variance of the random timing error per stage. This variance is a circuit-dependent parameter and is discussed in Chapter 5 and Appendix A. For the 5-delay-stage example,

$$S_X(\Omega) = \left[2 + \frac{12}{5}\cos(\Omega) + \frac{6}{5}\cos(2\Omega) + \frac{2}{5}\cos(3\Omega) \right] \cdot \sigma^2. \qquad (4 - 17)$$

Fig. 4.8 shows the plot of this function. This function maintains a constant at low frequencies and falls off as the frequency increases, shown in log-log plot. This unique phase noise profile is discussed in Section 4.4.

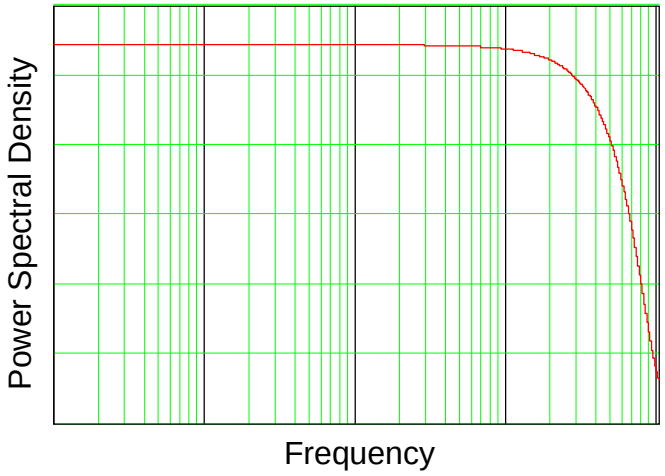

Fig. 4.8: Power Spectral Density for Five Delay Stage Example.

4.3.2 Spurious Tones

The other key performance specification for a frequency synthesizer is its spurious tone level. Spurious tones can be defined as systematic timing fluctuations in oscillation periods. In the time domain, the presence of systematic fluctuations in an oscillation waveform represents periodic timing errors. In the frequency domain, this manifests as undesired components in the frequency spectrum. There are wo major sources of spurious tones in a DLL-based frequency multiplier: *delay stage mismatches* and *static phase errors*.

Delay Stage Mismatch

When the DLL is in a perfect locked condition, the output waveforms of the DLL are evenly spaced within the reference period and the period of oscillation in the synthesized

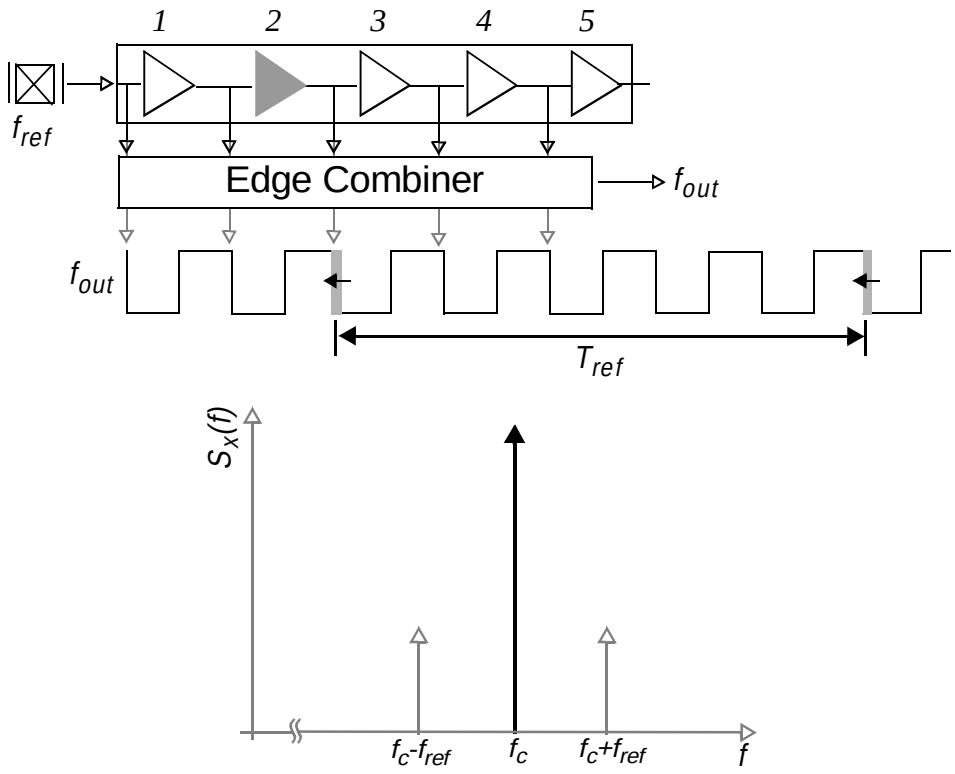

Fig. 4.9: Mismatch in Delay Stage.

output waveform is identical, this was shown in Fig. 4.2. In the frequency domain, the output spectrum is a single tone with phase noise around the center frequency.

However, if one of the delay stages has a mismatch (i.e., extra capacitance due to process variation or layout error), this causes the delay of this particular stage to be longer or shorter depending on the type of mismatch. For example, in Fig. 4.9, the delay *Stage 2* has a mismatch that causes its delay to be slightly *shorter* than others. The effect of this mismatch on the output waveform is that the output edge corresponding to the second DLL output is shifted *forward* by the same amount in time. Since the DLL is locked to one period of f_{ref}, this mismatch also occurs at the same frequency, f_{ref}, in the output wave-

form. Therefore, this systematic mismatches in the local oscillator output waveform give rise to spurious tones at f_{ref} and harmonics of f_{ref}. The closest spurious tones to f_c are located at f_{ref} away.

Mismatches in other parts of the DLL-based frequency multiplier can also cause spurious tones similar to the one mentioned above. For example, mismatches at the inputs of the edge combiner also have a similar spurious tone effect.

Static Phase Error

In a DLL, the phase detector senses the phase difference between input and output of the delay chain and generates a pair of UP/DN signals to control the charge pump output current. This charge pump output signal is filtered by the loop filter to create a control voltage for the delay chain. If the DC gain from the phase detector to the loop filter is finite, a phase difference at inputs of the phase detector is required to sustain the desired control voltage. This phase difference is generally known as the *static phase error*, shown in Fig. 4.10.

In the DLL-based frequency multiplier, the delay chain input and output waveforms should ideally be *in-phase*. The static phase error in a DLL represents a phase difference between input and output waveforms of the delay chain in a locked condition. For example, Fig. 4.10 shows the output waveform, f_V, leads the input waveform by a small margin. Because the synthesized output oscillations are triggered by the DLL output waveforms, an extended “blank” period is found at the end of each delay chain cycle

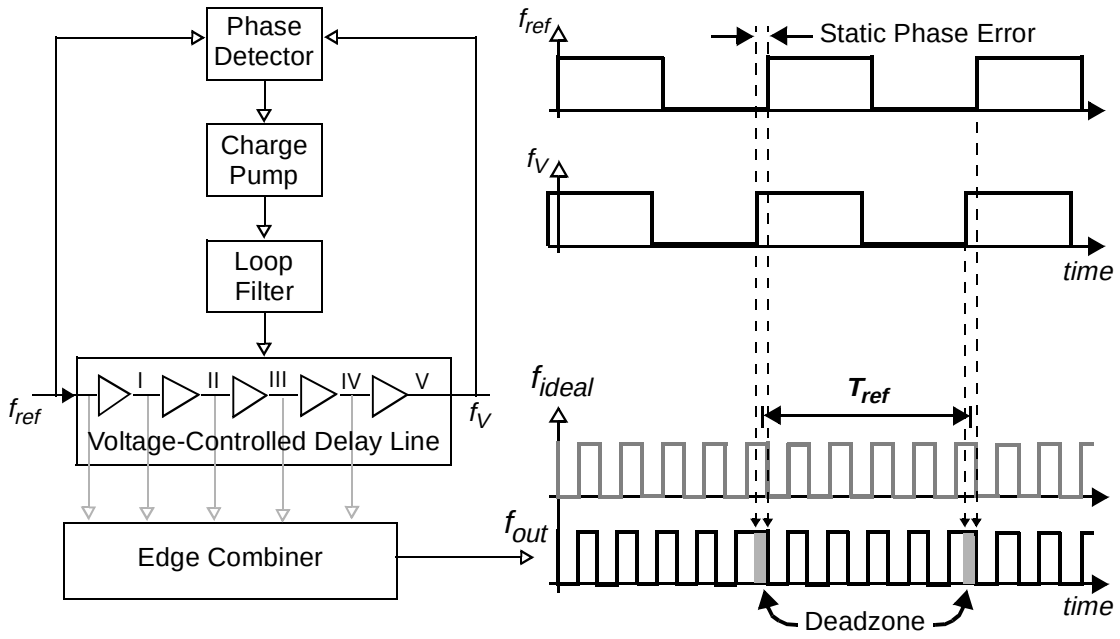

Fig. 4.10: Static Phase Error.

where the last oscillation completes and before the crystal reference starts the next cycle. This is commonly referred as the *deadzone*, also shown in Fig. 4.10.

The rate of occurrence for the deadzone is precisely, f_{ref}; hence similar to the delay-stage mismatch case, the static phase error also causes spurious tones to occur at f_{ref} and harmonics of f_{ref} where the closest spurious tones to f_c are located at f_{ref} away.

A common way to minimize the static phase error is to make the DC loop gain as large as possible. This can be achieved by properly selecting the loop filter topology (i.e., placing a pole at the origin). However, mismatches between UP/DN currents of charge pump and other non-idealities still cause static phase error. Fortunately, the spurious tones generated by the static phase error have the same characteristics as the delay stage mis-

match case. The next section presents methods to deal with this particular spurious tone pattern in wireless systems.

The conventional Phase-Locked Loop design also generates static phase error. Although there exists a slight phase difference between the reference crystal and output waveform in a PLL, since the desired output is the carrier frequency, its exact phase relationship to the crystal reference is not critical for most wireless communication applications.

4.4 Performance Implications for Wireless Communications

The previous section analyzed the two key performance measures, *phase noise and spurious tones*, for the DLL-based frequency multiplier. In the analysis, key contributors to the phase noise and spurious tones were described and their performance characteristics have been determined. In this section, a study of the phase noise and spurious tone performance characteristic is presented and their implications for the wireless communication systems is discussed.

4.4.1 Phase Noise

In Section 4.3.1, an extensive analysis was given to calculate the phase noise of the DLL-based frequency multiplier caused by the random timing errors in each delay stage. Because the random timing error for one delay stage is independent of other delay stages and does not accumulate from one delay chain cycle to the next, the correlation of timing

error random process suggests a particular phase noise profile which was shown in Fig. 4.8 for a five delay stage example. The general equation for a *N*-stage DLL was also given in Eq. 4 - 16.

Recall from Eq. 4 - 5, that the phase noise is a low frequency noise modulated up to RF frequency by the carrier frequency. Therefore, for low-frequency phase noise, it corresponds to the phase noise near the carrier frequency. In the 5-stage DLL example, the cosine terms in Eq. 4 - 17 equal to "1" for low frequencies; therefore, the phase noise is a constant near the carrier. As the offset frequency increases, the cosine terms start taking effect and the phase noise begins to decrease.

This phase noise profile agrees well with intuition. For the timing error correlation of two "distant" timing incidences (corresponding to a low frequency), since the random timing error does not carry over one delay chain cycle, the worst-case random timing error accumulation is one delay chain worth. This is shown as the flat region of the phase noise plot (Case 1 in Fig. 4.11). As the two timing incidences approach each other, the worst-case random timing error accumulation remains unchanged until the time difference between the two timing incidences becomes smaller than the period of the reference crystal. At this point, the random timing error accumulation becomes less and less as the two timing incidences approach each other within the period of the reference crystal frequency (equivalent to increasing the offset frequency). This can be seen as the phase noise rolls-off at higher offset frequencies (Case 2 in Fig. 4.11). A noticeable difference between

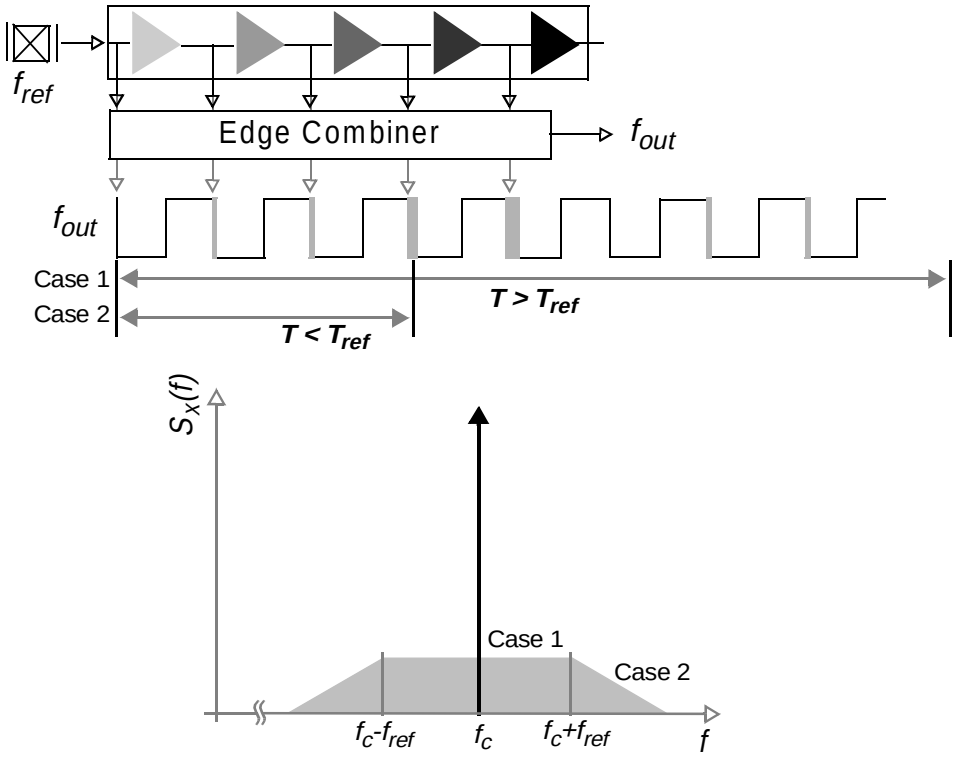

Fig. 4.11: Phase Noise Plot for Synthesized Delay Output.

the phase noise curve of the DLL approach compared with that of a conventional oscillator (shown in Fig. 2.15) is the flat region close to the carrier frequency vs. the typical oscillator phase noise shape.

This phase noise profile is especially attractive for modern cellular telephone applications. In order to increase the user capacity for a cellular basestation, the cellular telephone standard often requires the receiver to reject neighboring channels with a high signal power. Fig. 2.16 shows that the phase noise converts the adjacent channel power down to a lower frequency, and the down-converted term coincides with the desired channel. Therefore, close-in phase noise is required to be low to minimize the interference

from adjacent channels to the desired channel. The accumulation of timing jitter in a conventional PLL with a VCO causes the low frequency phase noise to be high. Furthermore, the low quality factor of integrated spiral inductors used in a monolithic VCO makes it even more difficult to satisfy the stringent cellular telephone requirements.

From the analysis in the previous section and the discussion above, the long term jitter performance for the DLL-based frequency multiplier is excellent due to the non-cyclical nature of random timing error accumulation. In addition, its phase noise only depends on the random timing error of the delay stage. Thus a DLL-based frequency multiplier provides with excellent close-in phase noise performance not attainable with a monolithic PLL implementation for narrow-channel cellular applications.

4.4.2 Spurious Tones

Section 4.3.2 describes the two main contributors to spurious tones for the DLL-based frequency multiplier, namely delay stage mismatch and static phase error. Due to the periodic nature of the delay chain, both contributors result in the same spurious tone characteristic where the closest spurious tones to the carrier, f_c, are located at $f_c \pm f_{ref}$. The system can only generate spurious tones at the integer multiples of the crystal reference frequency. This is because the functional blocks performing the frequency division do not exist in this architecture. Fig. 4.12 is a graphical representation of the spurious tone positions relative to the other features of the output frequency spectrum.

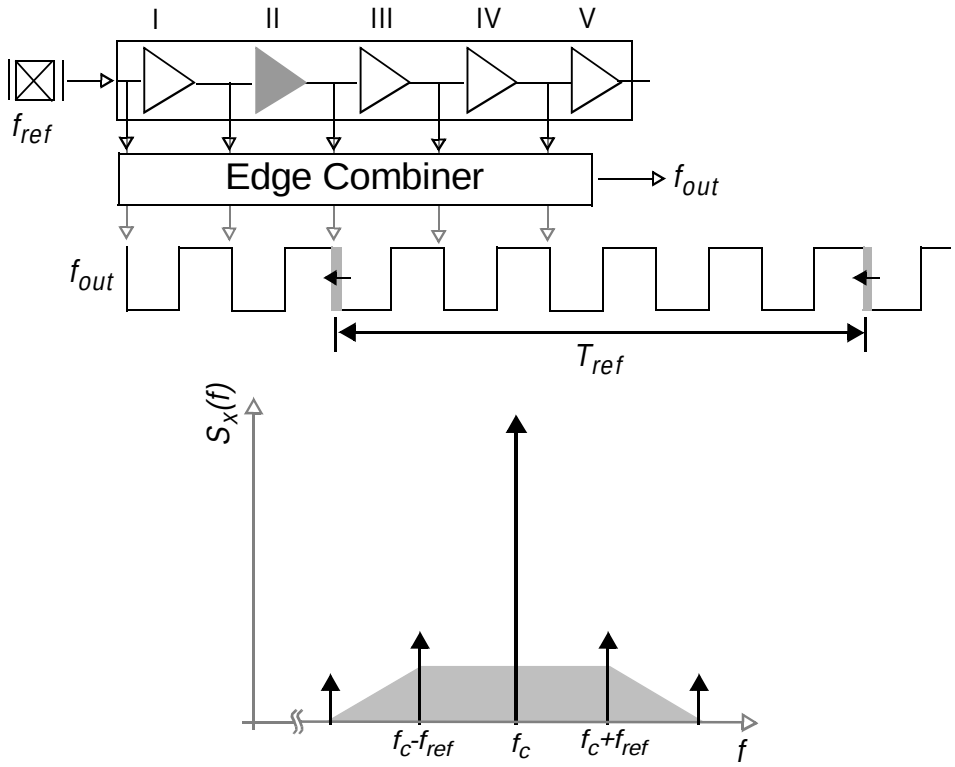

Fig. 4.12: Spurious Tones Locations.

Although mismatches are always present in an integrated circuit manufacture process due to lithography, process gradient, etc., by carefully choosing f_{ref}, the spurious tones for this approach can be placed strategically at frequencies6 that do not affect the radio system performance. Table 2-1 on page 9 shows that modern wireless communication standards all reside in a narrow RF frequency band compared with the carrier frequency. In almost all transceivers available today, a RF filter close to the antenna rejects signals outside of the frequency band for the receiver and/or to filter the PA output to avoid the spurious emission in a transmitter. When the spurious tones are located outside of the frequency band, the blocking requirement for receiver and spectral emission for transmitter are both greatly reduced.

Furthermore, some wireless standards allow a fixed number of spurious tone exceptions within the frequency band (i.e., GSM family allows six or twelve in-band and 24 out-of-band spurious tones - described in Chapter 2). Therefore, by carefully selecting the reference frequency, the spurious tones can be positioned far enough away from the center frequency (outside the band of interest) or strategically placed to satisfy the system requirements.

4.5 Summary

This chapter describes the fundamentals of a DLL-based frequency multiplier that include its concept, operation and implication in radio systems. The key performance difference between the DLL-based frequency multiplier and a conventional PLL with a VCO is that the random timing errors do not accumulate from one cycle of delay chain to the next in a DLL. This timing jitter accumulation pattern creates a correlation function that results in a unique phase noise profile. The phase noise profile is constant at low-offset frequency, which is the result of a good long-term random timing error performance. This feature is especially attractive for modern narrow-channel cellular telephone applications where a low phase noise is required at a close-in frequency. Monolithic implementations, using the conventional PLL approach, generally have a difficult time meeting the requirements for narrow channel spacing systems due to their high phase noise at a low offset frequency.

In addition to a good low-frequency phase noise performance, spurious tones also follow a well-defined pattern in the output spectrum. Due to the periodical nature of the delay chain, all spurious tones are harmonics of the crystal reference frequency. Therefore, the nearest spurious tones to the carrier are located at f_{ref} away. This simple and well-defined spurious tone pattern gives the radio system designer an extra degree of freedom for frequency planning during the system design.

The next chapter introduces the system design for the DLL-based frequency multiplier. The transfer function of each building block is derived, and the overall system equation will be analyzed. This will be followed by a description of the detailed circuit implementation for the low jitter delay stage with several design considerations particular to this LO. Control circuits (i.e., phase detector, charge pump and loop filter) and their design criteria will also be presented.

4.6 References

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Chapter 5

CMOS Local Oscillator Design using a DLL-based Frequency Multiplier

5.1 Introduction

The previous chapter presented a novel approach to implementing a low phase noise local oscillator. The concept of using the DLL-based frequency multiplier to generate a fixed-frequency LO was described and a five-delay-stage example was given. The unique jitter accumulation pattern provides good long-term timing error, which translates to excellent close-in phase noise performance. This concept was verified using a random process model. The analysis shows a constant phase noise profile for offset frequencies less than the input crystal reference frequency, and the phase noise decreases for frequency offsets beyond the reference frequency.

This chapter describes CMOS design techniques for DLL-based frequency multipliers. The system level design consideration is first introduced with a linearized small-signal AC model. In this model, transfer functions of each functional block and the overall system are defined; as well as the design techniques for each block are presented. Special attention is given to the delay stage because it is the main contributor of random timing

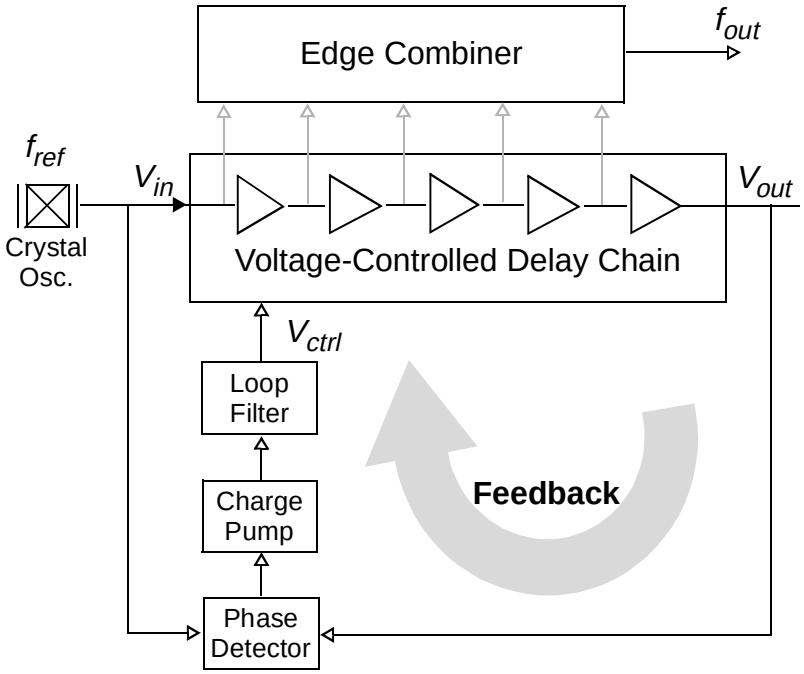

Fig. 5.1: Simplified Block Diagram for Delay-Locked Loop Frequency Synthesizer.

error in the delay chain, and it determines the performance of the local oscillator. The feedback-path components also play an important role in minimizing spurious tones in the output signal. Finally, the operation and design of the edge combiner, which accepts the delayed edges from the DLL and generates the final synthesized waveform, is discussed.

5.2 Small-Signal AC Model

Fig. 5.1 is a simplified block diagram of a DLL-based frequency multiplier. The phase detector accepts inputs from the V_{in} and V_{out} of the delay chain and outputs the phase difference. This phase difference output determines the charge pump action, and the loop filter averages the charge pump output. When the feedback is in place, the loop filter

outputs a control voltage which minimizes the phase difference at the inputs of the phase detector. In the steady state, the phase difference between V_{in} and V_{out} of delay chain is ideally zero. The edge combiner, which is not inside the DLL feedback loop, will not be included for this small-signal AC analysis.

5.2.1 Voltage-Controlled Delay Line

In the operation of a Delay-Locked Loop (DLL), the phase difference between V_{in} and V_{out} of the delay chain (in Fig. 5.1) are adjusted by the control signal, V_{ctrl}. If the crystal reference phase is fixed, to vary the phase of V_{out} with respect to the crystal reference phase, the time delay of the delay stage needs to be adjusted. The phase difference between V_{in} and V_{out} is equal to,

$$\phi_{diff} = \left[\sum_{i=1}^{N} \phi_i \right] - 2\pi \qquad (5 - 1)$$

The followings are three key characteristics required by the delay chain.

For the example in Fig. 5.1, when the DLL loop is in the locked condition, the crystal reference, V_{in}, and the output of the delay chain, V_{out}, are *in-phase;* or equivalently the sum of phase delays of all delay stages is exactly one period of the reference frequency by design. To generate the desired frequency using the edge combiner, the DLL output waveform edges are required to be *evenly* spaced within the reference frequency period. Therefore, all delay stages need to have an *identical* time/phase delay and to be adjusted

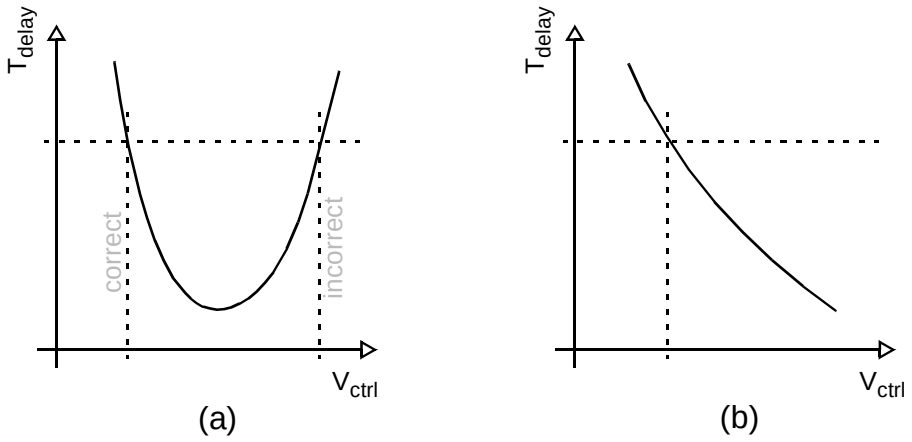

Fig. 5.2: Some possible Transfer Functions for DLL Frequency Synthesizer.

uniformly. This not only simplifies the design of the delay chain, but also minimizes the spurious tone component at the edge combiner output.

In the delay chain, the frequency of the propagating signal is already known, f_{ref}. Therefore, a simple phase detector can be used in place of the phase/frequency detector commonly found in a PLL. This may simplify the phase detector design complexity, however it imposes an additional constraint on the delay stage transfer function. In order for the DLL to properly lock to the correct edge, the delay chain transfer function needs to be monotonic within the tuning range, shown in Fig. 5.2. For example, if the delay per stage vs. V_{ctrl} follows the parabolic curve in Fig. 5.2a; two V_{ctrl}'s are possible for a given time delay and an incorrect locking condition may occur for the DLL. With a monotonic transfer function (Fig. 5.2b), a time delay corresponds to a single control voltage where no ambiguity is present. (In reality, a phase/frequency detector is still needed to detect the *phase offset*. See next section.)

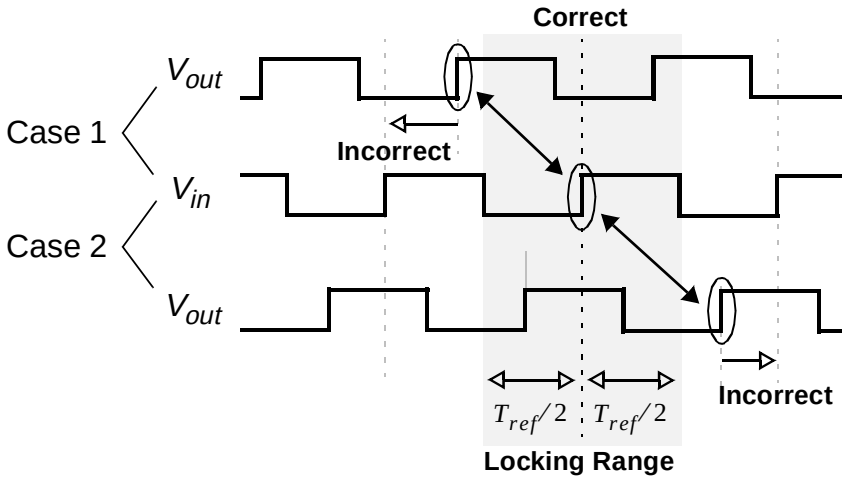

Fig. 5.3: Phase Detector Range.

Although the phase/frequency detector used in this implementation determines the phase *offset* between V_{in} and V_{out}, it does not always match corresponding edges from the correct V_{in} and V_{out} pair. For instance, in Case 1 of Fig. 5.3, if V_{out} is severely leading V_{in} by more than $T_{ref}/2$, the phase/frequency detector may determine that V_{out} is lagging the previous edge of V_{in} by less than $T_{ref}/2$ and try to adjust the control voltage to speed up the delay stages even further. The opposite can also happen when V_{out} is severely lagging V_{in} by more than $T_{ref}/2$, shown in Case 2 of Fig. 5.3. Therefore, to avoid the above situation, signals presented at the phase detector inputs need to be within a certain range, ideally within $\pm T_{ref}/2$, to guaranteed a correct phase detection. The total phase delay of the delay chain needs to be within $\pm\pi/2$ of the reference period by design including process variation.

Given the above characteristics, the transfer function for the delay chain is the input/output phase difference vs. the control signal, with the units $radians/volt$. Unlike the VCO

whose *s-domain* transfer function is K_{VCO}/s (phase is integral of frequency, in *s-domain* integral is *1/s*), the delay chain outputs the phase information directly. As a result, the transfer function for the delay chain is not frequency dependent. In addition, this transfer function needs to be monotonic as described earlier. Therefore, the transfer function is assumed to be a constant,

$$F_{VDL}(s) = K_{VDL}\left(\frac{radian}{volt}\right) \qquad (5 - 2)$$

Since the total phase difference is the sum of the total time delays of identical delay stages, this transfer function can also be written as a function of the time delay per delay stage vs. the control signal. This will be used for circuit design later in this chapter.

5.2.2 Phase Detector and Charge Pump

In the feedback control path, the phase detector and charge pump generally work together to convert the phase difference into an electrical signal that can be processed by later stages. In the DLL loop, if the crystal phase is used as a reference, the output of the delay chain can be either leading or lagging from the crystal reference phase, shown in Fig. 5.3. When the delay chain output is lagging the reference, the delay per stage needs to be shortened; on the contrary, when the delay chain output is leading the reference, the time delay needs to be lengthened (See Fig. 5.4). Therefore, the phase detector needs to distinguish not only the absolute *phase difference*, but also the *phase relationship*. Already

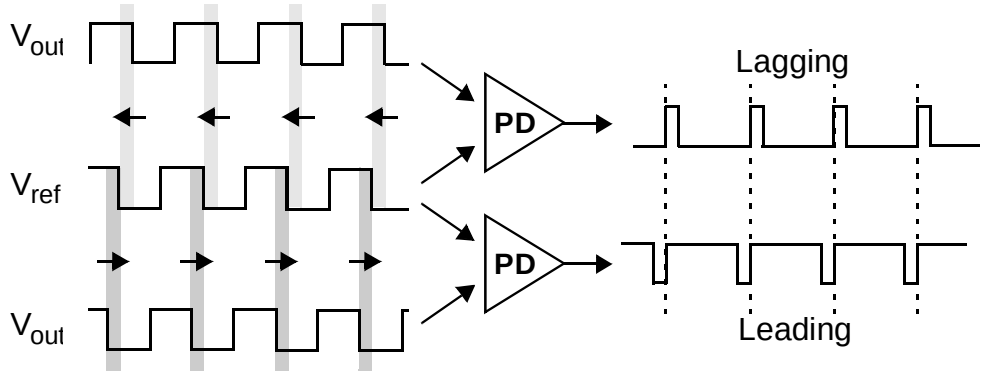

Fig. 5.4: Two Cases for Phase Detector to Resolve.

shown in Fig. 5.3, the inputs to the phase detector are required to be within $\pm\pi/2$ of the reference period for a correct phase detection.

After the phase detector determines the *phase offset*, it needs to be converted into an electrical signal which can be processed by later stages. Several methods are available to perform this function, while a common approach is to use a charge pump [73]. The idea of a charge pump is to deposit or withdraw charges to the output node according to the *phase offset* determined by the phase detector. This is accomplished by time-multiplexing charge pump currents in or out of the output node, and charges are deposited or withdrawn.

Therefore, the combined function of the phase detector and charge pump is to take a *phase difference* as an input and apply the charge pump current to the output for a portion of the period that is proportional to the *phase offset*. The combined transfer function is then

$$F_{PD-CP}(s) = K_{PD-CP} = \frac{I_{CP}}{2\pi} \left(\frac{amp}{radian}\right) \qquad (5 - 3)$$

where I_{CP} is the charge pump current, and the transfer function has the unit of $amp/radians$.

5.2.3 Loop Filter

The signal coming from the phase detector and charge pump combination has a large periodic content due to the recurring phase detection. To remove the high frequency component and average the charge pump output, a loop filter is applied at the output of the charge pump. This filter output is then used as the control voltage for the delay chain.

Unlike the static phase error in the PLL case, it results in large spurious tone components in the output of the DLL-based frequency multiplier. Therefore, an infinite DC gain in the loop filter transfer function is essential to minimize the static phase error. A typical loop filter for this application may have a transfer function,

$$F(s) = \frac{K_{LF}}{s} \qquad (5 - 4)$$

where K_{LF} is the loop filter gain and the integrator $1/s$ represents an infinite DC gain.

5.2.4 Overall DLL Transfer Function

The simplified block diagram of the DLL loop shown in Fig. 5.5a can be re-drawn with the small-signal AC transfer functions of the building blocks from the previous sections. This is shown in Fig. 5.5b. This figure can be easily recognized as a simple

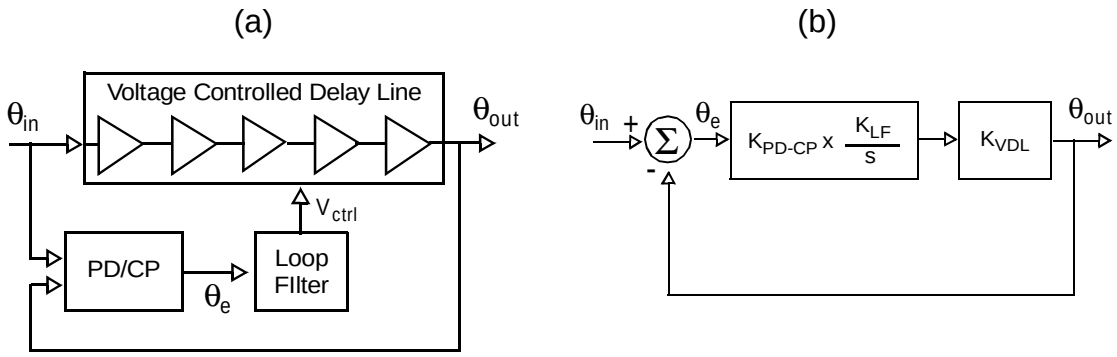

Fig. 5.5: Small-Signal AC Model of DLL Loop.

first-order feedback system. When the loop is in a steady-state locked condition, the *s-domain* phase transfer function from input to output is

$$\frac{\Phi_o(s)}{\Phi_i(s)} = \frac{G(s)}{1+G(s)} = \frac{K_{VDL}\cdot K_{PD-CP}\cdot K_{LF}/s}{1+K_{VDL}\cdot K_{PD-CP}\cdot K_{LF}/s} \qquad (5-5)$$

where

$$G(s) = K_{PD-CP}\cdot K_{LF}\cdot K_{VDL}/s \qquad (5-6)$$

is the loop gain of the DLL loop. With some simple algebraic manipulations, Eq. 5 - 5 can be re-written as

$$\frac{\Phi_o(s)}{\Phi_i(s)} = \frac{K_{PD-CP}\cdot K_{LF}\cdot K_{VDL}}{s+K_{PD-CP}\cdot K_{LF}\cdot K_{VDL}} \qquad (5-7)$$

This equation suggests a first order loop transfer function which is inherently stable. Unlike the small-signal AC model for a typical PLL, a minimum of a second order transfer function is required.

Since the transfer function is inherently stable, a wider loop bandwidth can be used. This allows a fast acquisition time, as well as the use of smaller loop filter capacitors facilitating integration. Similar to the PLL case, the small-signal AC model is only valid when the loop bandwidth is much smaller than the phase detector comparison frequency (generally 10:1). Therefore, the upper limit of the loop bandwidth is limited by the crystal reference frequency and is generally in the *MHz* range.

Assuming the DLL loop is ideal (with infinite bandwidth), which guarantees signals at V_{in} and V_{out} of the delay chain are perfectly *in-phase*, the thermal-noise-induced random timing error associated with each delay stage determines the noise performance of the local oscillator. In reality, the loop has a finite bandwidth which limits the loop response time. A slow acting variation in the control voltage which causes the *correlated* timing error for delay stages is quickly corrected by the loop. These variations generally prolong or shorten the time delay of delay stages *uniformly.* However, a fast acting variation whose frequency might be higher than the loop bandwidth is not corrected by the loop. These variations usually come from supply and control voltage noise. There also exists one case where the loop is not able to correct regardless of the loop bandwidth. When the timing errors for delay stages are *un-correlated* (shown in Fig. 5.6 where some random timing errors are longer and some are shorter), the total timing error at the output of the delay chain no longer carries the timing error information of each individual delay stage. Since the phase detector only detects the phase difference between V_{in} and V_{out} of

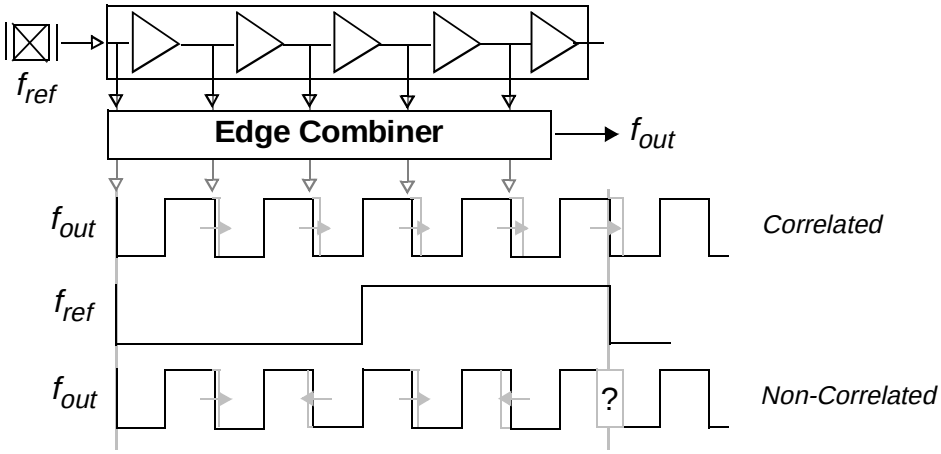

Fig. 5.6: Correlated vs. Uncorrelated Timing Error.

the delay chain, the loop is only able to correct the average timing error. This case generally occurs when the error sources are localized to the delay stage.

5.2.5 Edge Combiner

The last functional block before the RF output signal is the edge combiner. This block combines all the delayed edges from the DLL and generates a RF signal. Fig. 4.2 showed the basic operation of edge combiner, a more analytical approach is in this section [74].

Since the edge combiner function is to sum the various delayed versions of the input signal, V_{in}, its operation is similar to a *N*-tap Finite Impulse Response (FIR) filter model (Shown in Fig. 5.7 is a five-stage example). Each "D" block represents a delay stage in the delay chain, whose function is to delay the input signal, V_{in}, by $1/f_c$ (f_c is the output car-

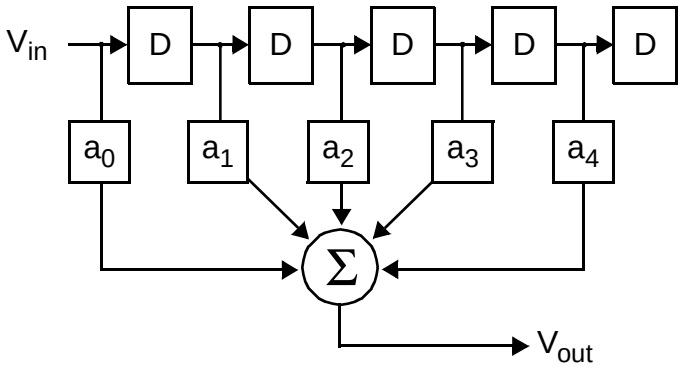

Fig. 5.7: Digital Filter Model for Five-Stage Delay Chain.

rier frequency). The output of the FIR filter can then be described using the following equation.

$$V_{out}(j\omega) = a_0 + a_1 e^{-j\omega/f_o} + a_2 e^{-j2\omega/f_o} + a_3 e^{-j3\omega/f_o} + a_4 e^{-j4\omega/f_o} \qquad (5 - 8)$$

where a_i 's are weighting coefficients in the digital filter. Assuming all the coefficients are unity, Eq. 5 - 8 can be written as

$$V_{out}(j\omega) = e^{-j2\omega/f_o} \cdot \left(e^{j2\omega/f_o} + e^{j\omega/f_o} + 1 + e^{-j\omega/f_o} + e^{-j2\omega/f_o} \right) \qquad (5 - 9)$$

and can be further simplified to

$$V_{out}(j\omega) = e^{-j2\omega/f_o} \cdot \left[1 + 2 \cdot \cos\left(\frac{\omega}{f_o}\right) + 2 \cdot \cos\left(\frac{2\omega}{f_o}\right) \right] \qquad (5 - 10)$$

The plot for Eq. 5 - 10 is shown in Fig. 5.8 where the y-axis is the magnitude and the x-axis is frequency normalized to f_o. The filter transfer function suggests that the DC and f_o components are enhanced, where as the frequencies at integer multiples of $f_o/5$ encounter nulls. In other words, for the DLL-based frequency multiplier, the harmonics of

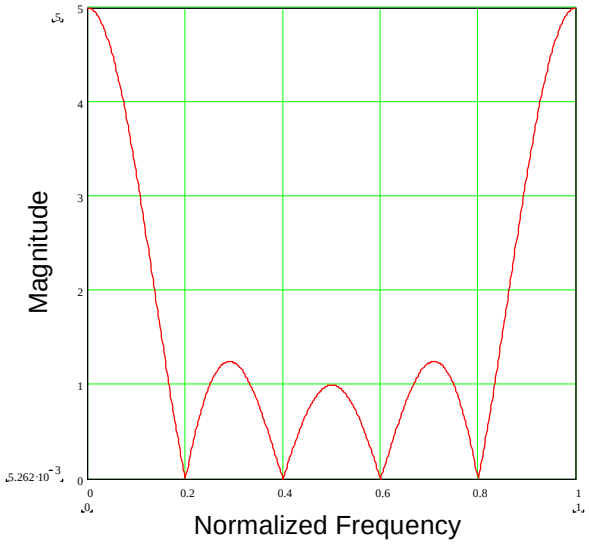

Fig. 5.8: Five-Tap FIR Filter Transfer Function.

the reference input frequency are ideally cancelled with the exception at $5 \times f_{ref}$ frequency, which is the desired output frequency in this example.

Therefore, by properly summing the DLL output waveforms, the desired LO output can be generated from the edge combiner. Since the edge combiner operation is completed outside of the DLL loop, there is no effect on the phase noise profile. However, depending on the circuit topology, it does contribute to some buffer phase noise to the final output. This will be discussed in Chapter 6.

5.3 CMOS Delay Stage Design

The analysis in the previous chapter indicated that the majority of the phase noise comes from timing uncertainties in the delayed edges. A great deal of attention is devoted

to the delay stage design, not only to ensure the proper DLL operation, but also to minimize its noise contribution. This section begins with a basic delay chain design which complies with the requirements described in Section 5.2.1. It is followed by a detailed explanation of the specific design parameters, such as the voltage swing, voltage gain and delay variation.

5.3.1 Basic Delay Chain Design

The delay chain consists of cascaded delay stages. Although the total time delay of the delay chain can be adjusted by varying the phase of one delay stage, as described in Section 5.2.1, the delay stages within the delay chain are identical and need to be adjusted uniformly. Identical delay stages also offer a larger phase tuning range at the delay chain output to accommodate a wider output frequency range.

Fig. 5.2 shows that the delay chain transfer function needs to be monotonic to avoid the incorrect DLL locking condition. The individual delay-stage transfer function also needs to be monotonic with the same transfer function since the phase difference between v_{in} and v_{out} and the phase delay per stage relationship is described in Eq. 5 - 1. The overall delay chain transfer function can be written in terms of the single delay-stage transfer function (i.e., time delay per stage vs. control voltage).

Given the above two requirements, a basic differential delay stage consisting of a NMOS input differential pair with triode-region PMOS loads is chosen for its process independence and simplicity in the delay control. Its circuit schematic is shown in Fig. 5.9

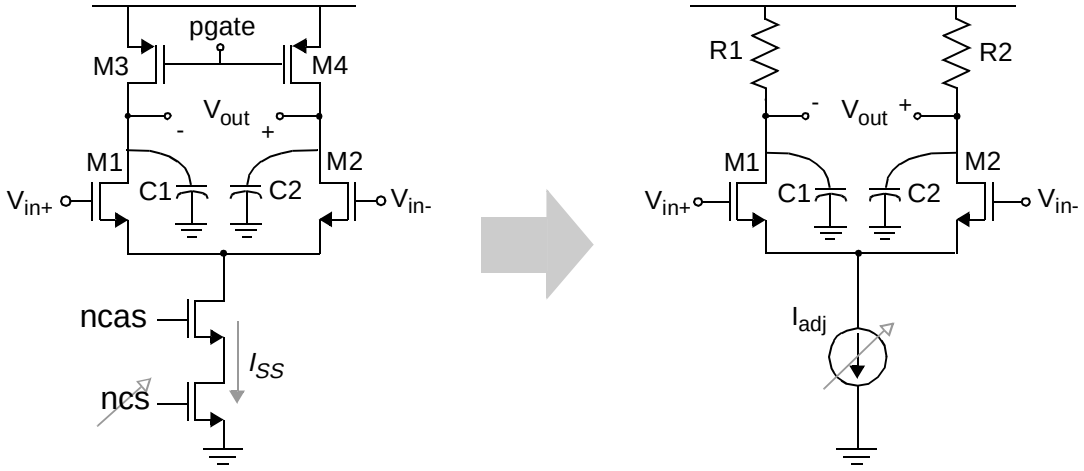

Fig. 5.9: Differential Delay Cell with PMOS Triode Load.

and a similar delay stage was used in [75][76]. Extra capacitors are added at the output nodes to achieve the desired delay per stage for a given application. Assuming the capacitive loading at the output is approximately constant, the delay per stage can be adjusted by varying the current source with a control voltage. The next three sub-sections will focus on the discussion of the design parameters for this circuit in terms of the voltage gain, voltage swing, and replica bias circuits.

5.3.2 Interstage Gain Consideration

In designing cascaded delay stages, it is essential to maintain the signal level throughout the entire delay chain. To achieve that, a sufficient gain per stage is required. Assuming the single-ended voltage swing is V_{SW} and the current source is I_{SS}, the small-signal gain per stage can be expressed as

$$a_v = g_m \cdot R_L = \frac{2 \cdot (I_{SS}/2)}{V_{GS(N)} - V_{TN}} \cdot \frac{V_{SW}}{I_{SS}} = \frac{V_{SW}}{V_{GS(N)} - V_{TN}} \quad (5 - 11)$$

where R_L is the equivalent resistance of the triode region PMOS device. In order to maintain the signal level, the gain per stage has to be greater than one, $a_v > 1$. This suggests that $V_{SW} > V_{GS(N)} - V_{TN}$. On the other hand, a higher gain amplifies the thermal noise from the previous stage and increases the timing error. Therefore, the gain is kept as small as possible with a sufficient safety margin to satisfy $a_v > 1$ within some process variation tolerances.

Since the lower bound for $V_{GS(N)} - V_{TN}$ is set by the random timing error requirement (See Appendix A), this determines the minimum V_{SW} allowed. In general, with the consideration of the design safety margin, V_{SW} is required to be 50-70% higher than $V_{GS(N)} - V_{TN}$. So the gain, a_v, is roughly 1.5 - 1.7. The design considerations for V_{SW} will be discussed in the following section.

5.3.3 Voltage Swing Consideration

The choice of the output voltage swing in the differential delay stage with triode region PMOS loads is influenced by many factors. To generate a high output frequency from the DLL-based frequency multiplier, t_{delay} per stage needs to be small. In the first-order model, t_{delay} can be approximated as

$$t_{delay} = \frac{C_L \cdot V_{SW}}{I_{SS}} \quad (5 - 12)$$

where C_L is the capacitive loading at the output node. Assuming C_L and I_{SS} are fixed for a particular design, t_{delay} will be linearly proportional to V_{SW}; and a small V_{SW} will result a small t_{delay}. On the other hand, a small V_{SW} may not be able to switch the subsequent differential stages completely. The differential input voltage required to fully switch a NMOS differential pair is approximately $\sqrt{2}$ times the balanced $V_{GS(N)} - V_{TN}$ of the input devices [77]. Also, a small V_{SW} is more susceptible to the thermal noise problem in the delay stage.

Already seen in the previous section on the delay stage *gain*, V_{SW} is required to be larger than $V_{GS(N)} - V_{TN}$. For the DLL-based frequency multiplier, the outputs of each delay stage is used to drive the edge combiner inputs. Although buffers are placed between the delay chain and the edge combiner, a large swing is still required to ensure the proper operation for the edge combiner. Ideally, a rail-to-rail swing, $V_{SW} = V_{CC}$, is desirable.

There are other considerations that limit the upper bound for V_{SW}. In this differential delay stage design (Fig. 5.9), PMOS load transistors must be kept in the triode region for the entire phase tuning range. In order to achieve this, the source-drain voltage of the PMOS has to be less than the device gate overdrive,

$$V_{DS(P)} = V_{SW} < V_{GS(P)} - V_{TP} \tag{5 - 13}$$

The range for $V_{GS(P)}$ can be close to the full supply voltage, and therefore, upper bound for V_{SW} is set by $V_{DD} - V_{TP}$. For example, with a 3.3V supply voltage and a PMOS thresh-

old voltage of 0.7V, V_{SW} can be as large as 2V. In practice, the PMOS load device is generally kept *well* inside the triode region over the full voltage swing range to ensure a relatively-constant channel resistance. Hence, the *-3dB* frequency of the delay stage does not vary greatly due to the PMOS load variation.

In addition to the triode region PMOS load devices, NMOS input differential pair devices are required to remain in the saturation region throughout the voltage swing range. For device *M1* in Fig. 5.9, when input is at 3.3V supply, the drain-source voltage of *M1* can be small enough to push the device into the triode region and lose the current gain, g_m. To avoid this, the following condition needs to be met,

$$(V_{CC} - V_{SW}) - V_{S(N)} > (V_{CC} - V_{S(N)}) - V_{TN} \tag{5 - 14}$$

or equivalently,

$$V_{TN} > V_{SW} \tag{5 - 15}$$

The V_{TN} in the above equation is heavily influenced by the body effect since the source potential is $V_{GS(N)}$ below the input voltage, however well above the substrate potential.

Taking into account the considerations described above and the previous section, V_{SW} is chosen to be around 1V where the PMOS load devices can be comfortably in the triode region, and the $V_{GS(N)} - V_{TN}$ of the differential pair input devices also satisfies the requirements for noise and gain.

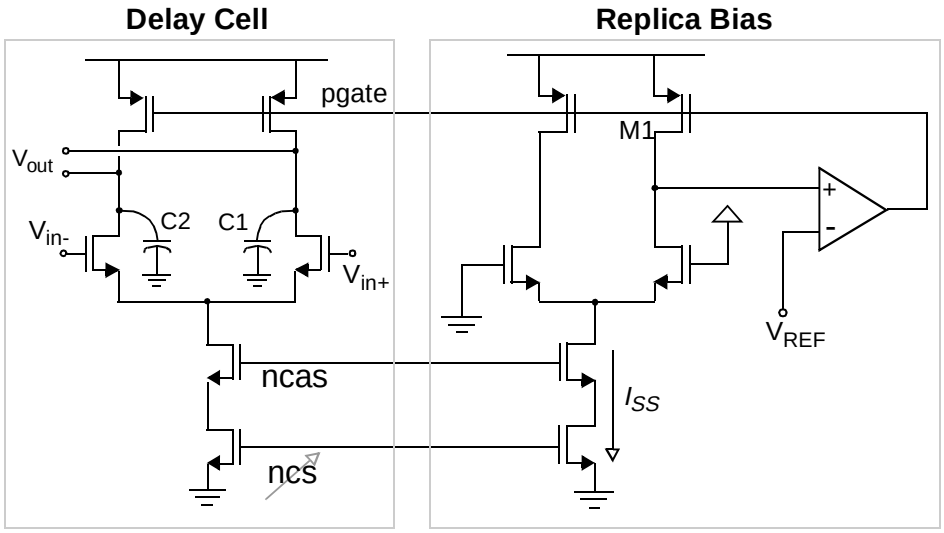

Fig. 5.10: Conceptual Diagram for Replica Bias.

5.3.4 Replica Bias Circuit

Fig. 5.2 suggests that to achieve proper locking condition in the DLL, monotonicity is required in the delay chain transfer function. Eq. 5 - 12 indicates t_{delay} and I_{SS} are inversely proportional to each other if V_{SW} and C_L are fixed. Because of the extra added capacitors, C_L, is roughly a constant; therefore, it is important to keep V_{SW} constant for different values of I_{SS} to ensure the monotonicity for the delay stage transfer function.

Since $V_{SW} = I_{SS} \cdot R_L$, variable-resistance triode region PMOS devices, *M3* and *M4* in Fig. 5.9, are used as the loads, R_L, to maintain a constant V_{SW} for the differential delay stage. Fig. 5.10 shows a conceptual block diagram of the replica bias circuit which adjusts the PMOS gate voltage with a feedback loop to keep V_{SW} a constant. This technique was introduced by B. Kim for use in the disk drive clock recovery PLLs [75][78][79]. In the replica bias circuit, a “replica” delay stage circuit is used along with an OpAmp. The tail

current, I_{SS}, is equal to the current in delay stages and V_{REF} is equal to $V_{CC} - V_{SW}$. The feedback forces the drain voltage of *M1* to be equal to V_{REF} for a given I_{SS} by adjusting the *M1* gate voltage. When the current in the delay stage changes to accommodate a different phase delay requirement, I_{SS} is changed accordingly. The replica bias sets up a new *M1* gate voltage which ensures the same V_{SW}. This then achieves the monotonicity according to Eq. 5 - 12. Another important consideration for the use of replica bias is to ensure the swing is relatively insensitive to process variation [80].

The OpAmp specification for this application is relatively simple. Since the accuracy requirement is relatively-relaxed for the replica bias circuit, a reasonable DC gain for the OpAmp is sufficient. The control voltage which varies the tail current had been filtered by the loop filter, hence, no high frequency component is present. The OpAmp -3dB bandwidth only needs to be on the order of the loop filter bandwidth.

5.3.5 Implementation

Fig. 5.11 shows the detailed circuit schematics of the delay stage with the replica bias circuit. The voltage swing chosen is 1V (2.3 - 3.3V) across the PMOS load device and no level shift is required between the delay stages. Extra poly-poly capacitors are introduced at the output nodes to achieve the proper time delay (shown as C1 and C2). Time delay for each delay stage is adjusted through the NMOS current source. Devices *M1*, *M2* and *M3* in replica bias are identical to the corresponding devices in the delay stage. *M1* mirrors the current source from the delay stage and *M3* sets up the V_{SW} across its

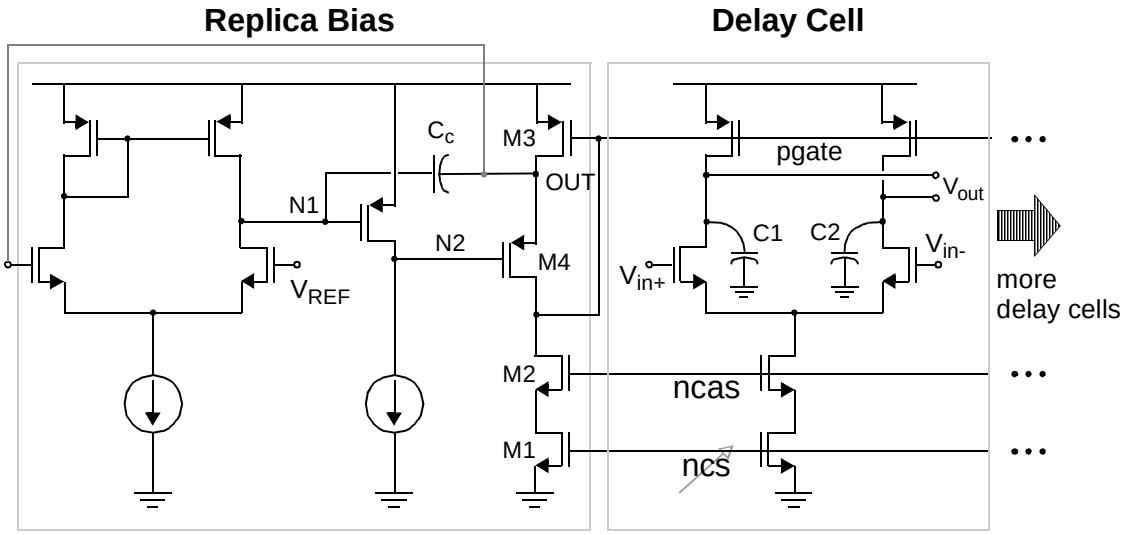

Fig. 5.11: Circuit Schematic for Delay Cell and Replica Bias.

source-drain. A PMOS source follower M4 is inserted between the triode load and current source device for the following two reasons,

1. For circuit configuration in Fig. 5.10, if the PMOS load device, *M1*, enters saturation region during transient, the replica bias loop gain may increase to a point where the loop becomes unstable. In Fig. 5.11, this problem is alleviated by connecting *M3* gate to *M4* drain to ensure *M3* in triode region during the transient.

2. Large load capacitance is found on PMOS gate since it is used to connect to all the PMOS load devices in the delay chain. For configuration in Fig. 5.10, the large capacitance will load the OpAmp output considerably. In Fig. 5.11, by inserting M4, it acts as a source follower buffer to the OpAmp output and the large capacitance of the PMOS gate node does not affect the OpAmp pole location to the first order.

The OpAmp topology used is a simple two stage configuration with the pole splitting compensation. The compensation capacitor, C_C, is connected between the node N1 and OUT to take advantage of the low impedance at OUT and move the feed-forward zero to a higher frequency. Similar OpAmp topology can be found in [77] and other references.

5.4 Control Circuitry Design

Although the major noise contribution in the DLL-based frequency multiplier comes from the random timing error in the delay stages, the feedback control circuits are important to ensure a correct operation of the DLL. The feedback path consists of phase detector, charge pump and loop filter. All of these blocks work together to implement the desired transfer function.

5.4.1 Phase Detector

Phase detector (PD) which senses the phase difference between the input and output of the delay chain performs a critical function to ensure the correct DLL operation. The accuracy of the phase detection determines the spurious tone magnitude. Existing phase detectors include Gilbert multiplier, double-balanced multiplier, triangular phase detector, etc. In this application, a tri-state phase/frequency detector is chosen for its operation with the charge pump.

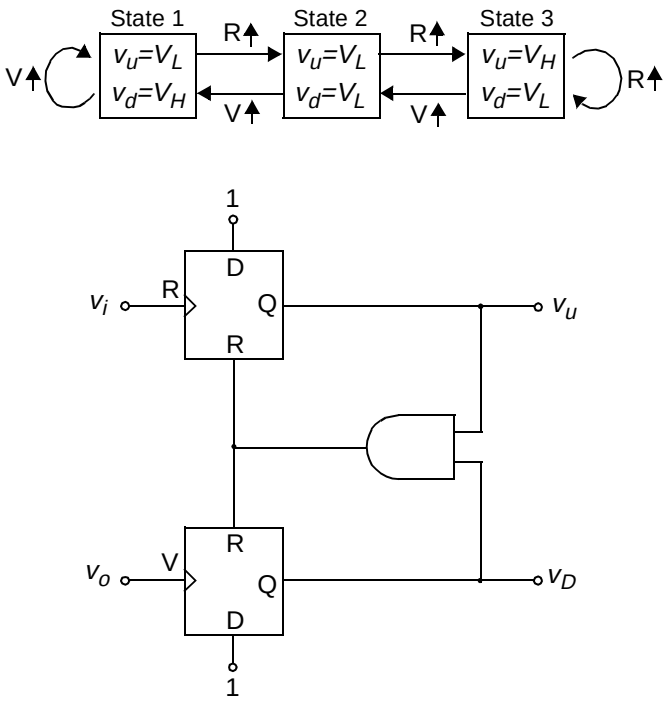

Fig. 5.12: Tri-State Phase Detector.

Fig. 5.12 shows the state and logical block diagram of a tri-state phase/frequency detector [81]. With three states, this phase detector can detect both phase and frequency. Although both inputs to the phase detector for this application are at the same *frequency,* a tri-state phase detector is still chosen for its ability to distinguish the two cases shown in Fig. 5.4. Assuming the flip-flops are triggered on the rising edge, v_i will cause the v_U (UP) waveform to rise and v_o will cause the v_D (DN) waveform to rise. When both v_U and v_D are high, the *AND* gate resets the flip-flop and both v_U and v_D are brought back to zero immediately.

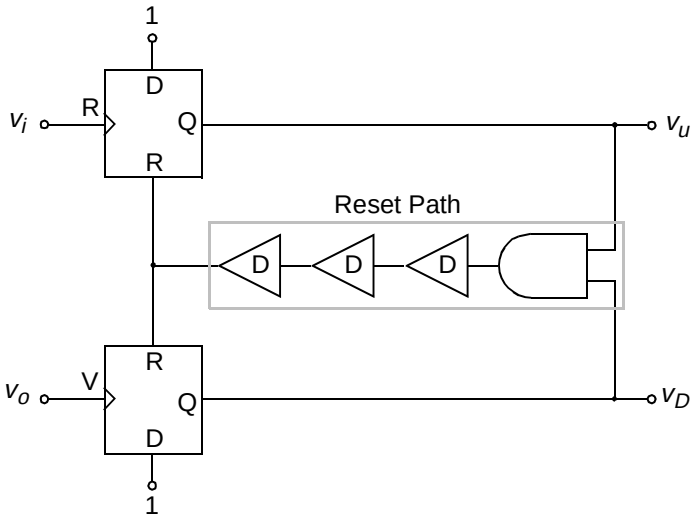

Fig. 5.13: Tri-State Phase Detector with Extra Delay in RST Path.

This phase detector generates two pulses whose pulse width difference is ideally equal to the phase difference of the input signals. Depending on the time delay of the reset path, the shorter pulse might be a small spike due to the finite rise and fall time in logic gates. In order to achieve a better matching between UP/DN pulses, extra delays are inserted in the reset path (shown in Fig. 5.13) to increase both pulses' widths by the same amount. The upper limit for the extra added delay in the reset path is the noise performance. These two signals are used in the charge pump to convert the phase difference information to an electrical signal.

The complete implementation of the phase/frequency detector is shown in Fig. 5.14[1] [82]. The flip-flop's are implemented with cross-coupled OR gates and each gate uses DCVSL topology shown in Fig. 5.15. DCVSL gates are chosen because of the rail-to-rail

1. In Fig. 5.14, IN is for the delay chain input signal and OUT is for the delay chain output signal.

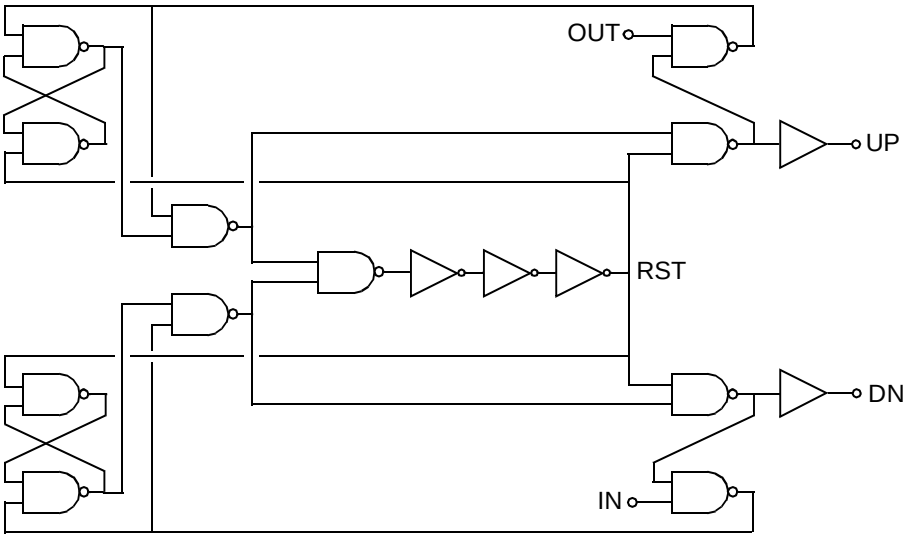

Fig. 5.14: Circuit Schematic for Phase Detector.

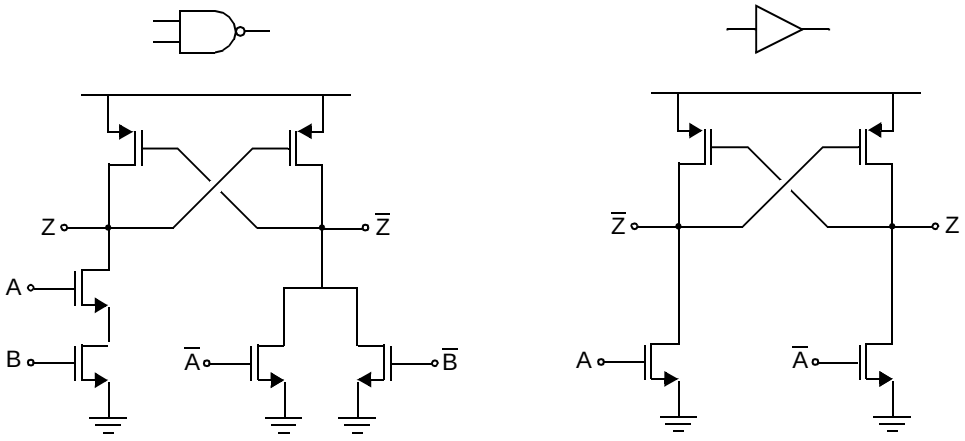

Fig. 5.15: DCVSL NOR Gate and Buffer Circuits.

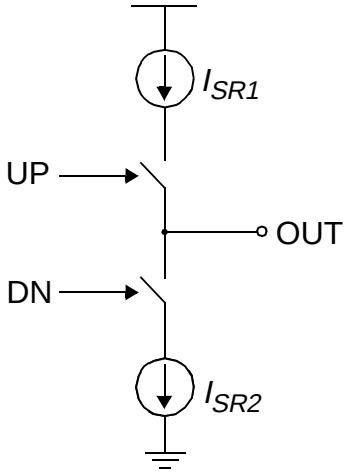

Fig. 5.16: Conceptual Circuit Diagram for Charge Pump.

positive latch action for a fast rise/fall time. Complimentary outputs, which are required for the charge pump operation, are also available with the DCVSL topology.

5.4.2 Charge Pump

The use of a charge pump in the PLL was first introduced by Floyd M. Gardner [73] and has been widely used in PLL and DLL applications. Fig. 5.16 shows the conceptual diagram for a charge pump. The UP/DN signals generated by the phase detector are used to time-multiplex the currents from the current sources, I_{SR1} and I_{SR2}, into the output node. Assuming that $I_{SR1} = I_{SR2}$, and the UP/DN pulse shapes and switches are ideal, the pulse width difference between the UP and DN signals is proportional to the charges deposited and withdrawn at the output node. For example, if inputs to the phase detector are perfectly *in-phase* and the UP/DN signals are identical, the current measured at the output node would be ideally zero. On the other hand, if the inputs to the phase detector are not *in-phase*, the average current measured at the output is $\frac{I_{SS}}{2\pi} \cdot \theta_e$, where θ_e is the

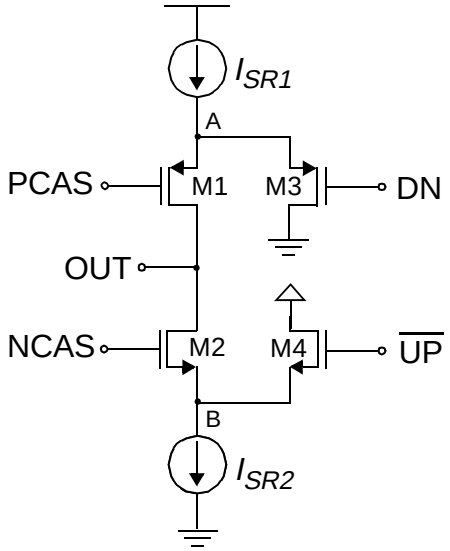

Fig. 5.17: Simple Charge Pump Circuit.

phase difference between the two inputs to the phase detector. Therefore, the combined transfer function for the phase detector and charge pump is

$$K_{PD-CP} = \frac{I_{SS}}{2\pi} \tag{5 - 16}$$

One important aspect in the charge pump design is to minimize the dynamic mismatch between the UP and DN currents. The dynamic mismatches mainly arise from the asymmetry in rise and fall times of UP/DN signals, as well as the difference in the electron mobility for NMOS/PMOS. Shown in Fig. 5.17 is a simple charge pump circuit schematic. When *M3* and *M4* are on, the *UP/DN* currents are drawn away from the output node; while *M3* and *M4* are off, the *UP/DN* currents are applied to the output node. A careful examination suggests that nodes *A* and *B* experience large voltage swings during the charge pump cycle. This causes a current mismatch at the output due to the different

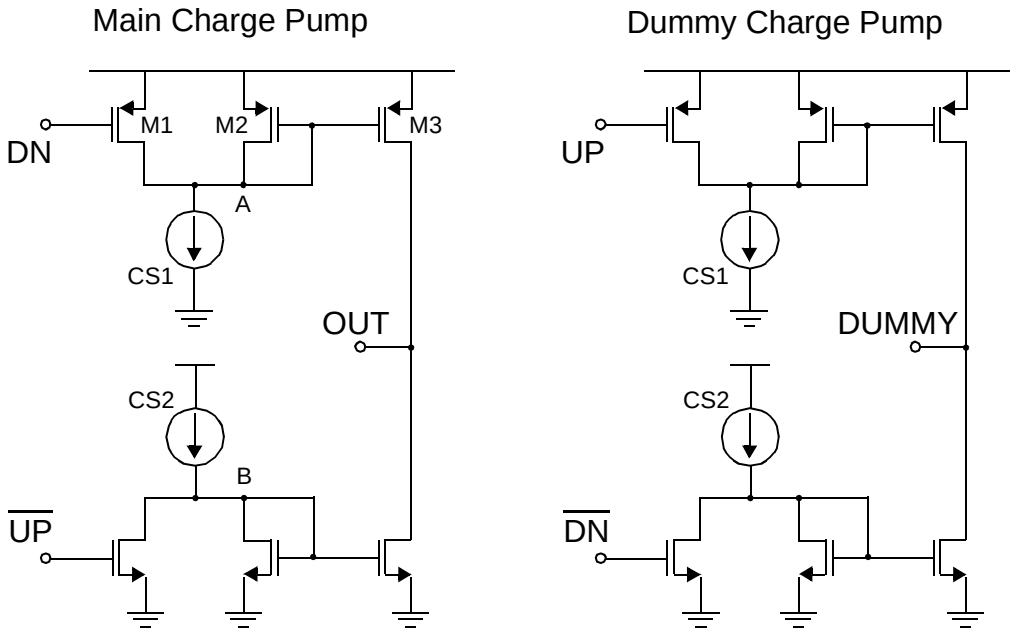

Fig. 5.18: Circuit Schematic for Charge Pump.

recovery time on nodes A and B. Furthermore, if the node A potential is below the output voltage when *M3* is on, a reverse current flow may discharge the output node (vice versa for node B). The dynamic mismatch needs to be compensated by a static phase error at the PD input which translates to spurious tones in the overall output. In DLL frequency multiplier application, the static phase error must be minimized.

Knowing the dynamic mismatch problem described in Fig. 5.17, a charge pump circuit with small internal node voltage variations is shown in Fig. 5.18 [83]. When DN is high, the current, CS1, is mirrored through M2 and M3 to the output and the voltage at node A is $V_{GS(P)}$ below V_{DD}. When DN is low, the current, CS1, is directed to the supply and the voltage at node A is roughly $V_{DS(P)}$ below V_{DD}. In the same way, node B also experiences a smaller voltage variation during the UP/DN cycle. Hence, this charge pump

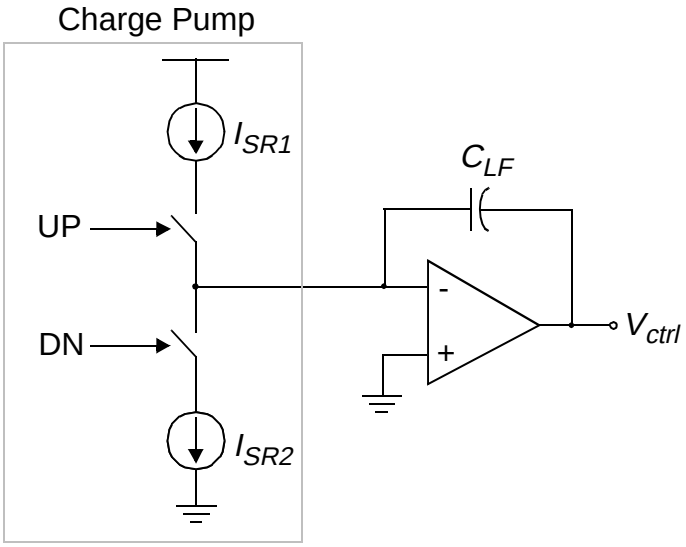

Fig. 5.19: Loop Filter Configuration.

configuration achieves a better dynamic current matching than the one in Fig. 5.17. A replica charge pump is used to ensure identical loading on both UP/DN, $\overline{UP}$/$\overline{DN}$ PD outputs.

5.4.3 Loop Filter

The function of a loop filter is to remove the high frequency components in the charge pump output and produce a control voltage to adjust the current sources in the delay stages shown in Fig. 5.9. From the previous chapter, it has been shown that an infinite DC gain in the loop filter transfer function minimizes the static phase error. Furthermore, to minimize the effect of early voltage or the λ effect in the charge pump output, an active circuit is used to keep the charge pump output voltage relatively constant during the transient. This results in a better current matching, hence reduces the static phase error. The above two requirements suggest a loop filter configuration which is shown in Fig. 5.19.

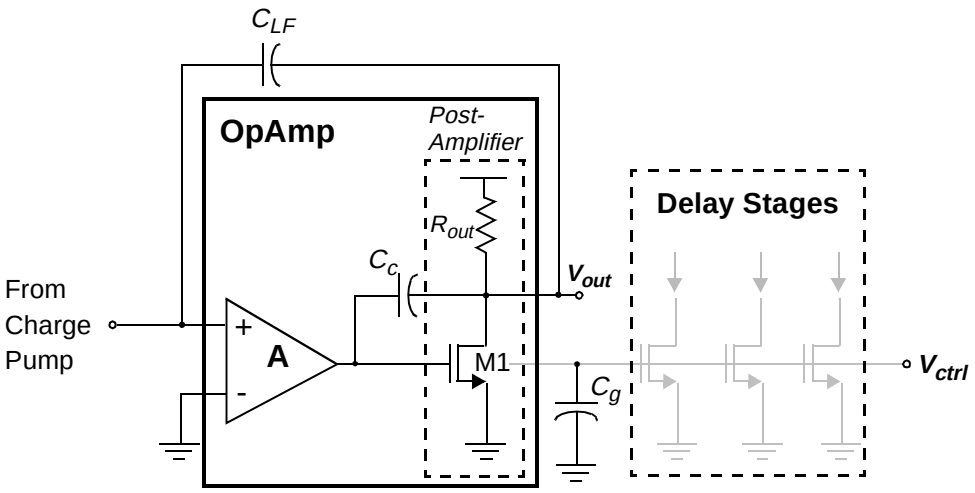

Fig. 5.20: Modified Loop Filter Configuration.

The capacitive input guarantees an infinite loop gain at DC, and the active loop filter produces a virtual ground node at the charge pump output. The output of the loop filter controls the current source devices and varies the tail current until a locking condition is achieved. Due to the large number of delay stages in the delay chain, when the loop filter output is connected to the current sources directly, a large capacitive load is present. This reduces the filter bandwidth considerably. To mitigate this effect, the large gate capacitance is incorporated into the loop filter design as shown in Fig. 5.20. Transistor *M1* is designed to have the reference current for the delay stage current sources. The resistive-loaded low-gain "post-amplifier" enables the non-dominant pole to be at a high frequency, while the dominant pole is formed by the gate capacitance, C_g, of the delay stage current source devices. The pole-splitting compensation capacitor, C_c, moves the non-dominant pole to an even higher frequency to ensure its effect on the OpAmp is negligible. When the feedback is in place, the bandwidth is increased by the OpAmp DC gain

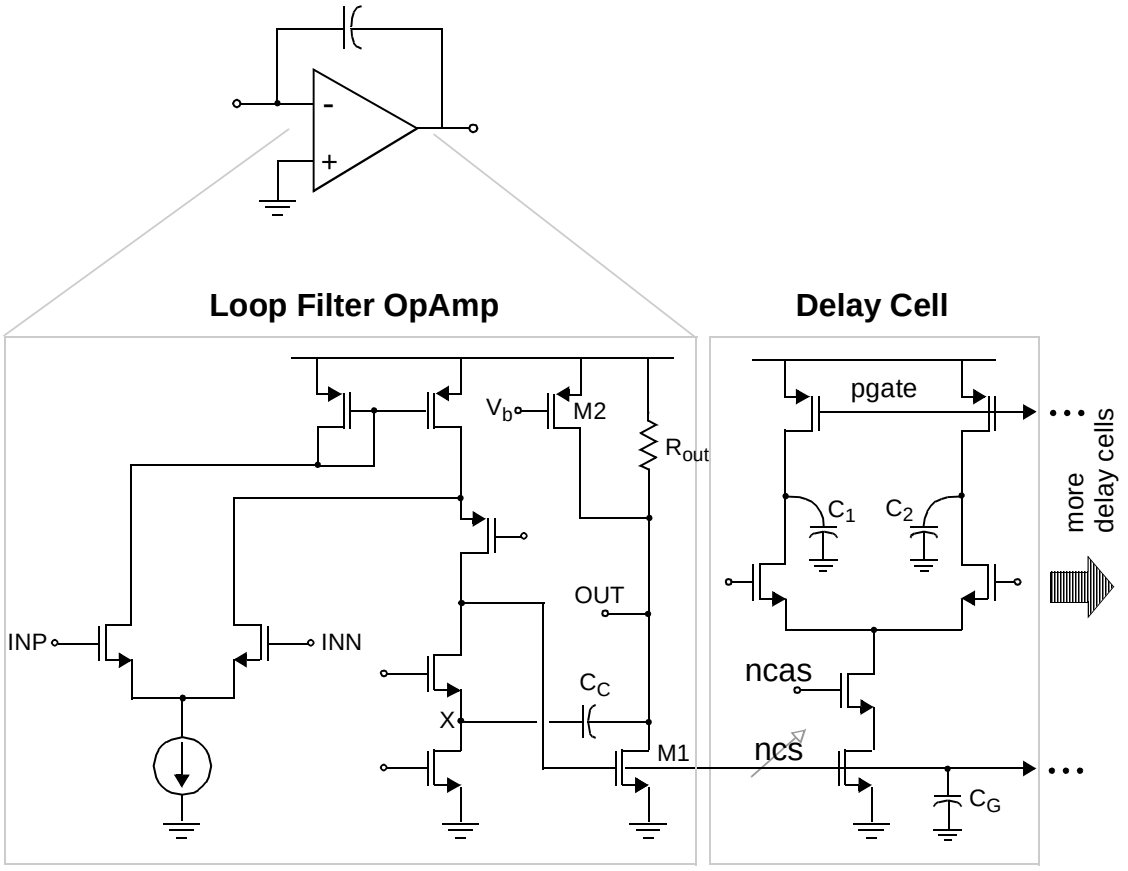

Fig. 5.21: Circuit Schematic for Loop Filter.

and the DC output voltage is determined by the dynamics of DLL loop. The voltage drop across the resistor, R_{out}, determines the current required for the delay stages to achieve a locking condition. This current is mirrored to the delay stage current sources via *M1*. The process variation of the resistor is taken into consideration in the prototype implementation.

Fig. 5.21 shows the complete circuit schematic for the loop filter OpAmp. The main OpAmp uses a folded cascode topology [77] with NMOS inputs. “Post-amplifier” is the same as what was described in Fig. 5.20 where *M1* is designed to have the reference cur-

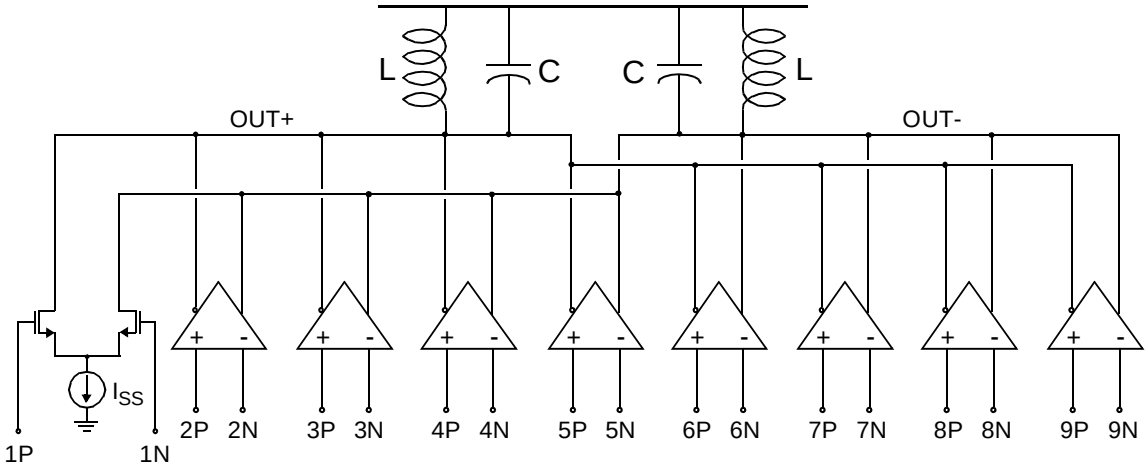

Fig. 5.22: Circuit Schematic for Edge Combiner (N=9).

rent for the delay stage current sources. The compensation capacitor is placed between the output node and node X to avoid the feed-forward zero in the standard Miller compensation. A controlled high-ohmic poly resistor is used for R_{out} with the consideration of process variation and locking range. Current source device M2 provides roughly half of the desired current to ensure a proper start-up condition.

5.5 Edge Combiner

It is clear from the discussion in the previous chapter that the function of an edge combiner is to take the outputs of the DLL and generate a RF frequency. It has been shown in Section 5.2.5, by properly summing the delayed output signals, unwanted harmonics are cancelled ideally.

Fig. 5.22 shows the circuit schematic for the edge combiner. The circuit consists of *N* differential pairs (where *N* is the number of stage or the multiplying ratio) and each is driven by an output from the delay chain. In addition, two spiral inductors are used to tune out the drain parasitic capacitance associated with the NMOS differential pairs. Since the outputs from delay chain are spaced evenly within the reference period, they time-multiplex the currents, I_{SS}, into the LC-tanks. From the *N*-tap FIR filter analysis shown earlier in this chapter, a differential current, $\pm I_{SS}$, can be found toggling between the +/- output nodes at the desired local oscillator frequency. The output swing is roughly equal to $I_{SS} \cdot (Q^2 \cdot R_{eq})$ where Q is the quality factor and R_{eq} is the equivalent series resistance of the spiral inductor. The output DC point is around $V_{CC} - \left[\frac{(N-1)}{2} \cdot I \cdot R_{eq}\right]$. The example shown in Fig. 5.22 where $N = 9$ is the actual implementation of the edge combiner in the experimental prototype. This will be described in more detail in Chapter 6.

5.6 Summary

In this chapter, the system level design consideration was first introduced with a linearized small-signal AC model. The transfer function for each individual block was derived and implemented in the system model. The CMOS design techniques for the key building blocks were presented with a special attention on the delay stage. In the next chapter, a brief summary about the target cellular system will be discussed, followed by a detailed description of the prototype implementation and the overall performance estimation.

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Chapter 6

Prototype Implementation

6.1 Introduction

As a demonstration of the DLL-based frequency multiplier technique, a fully integrated CMOS local oscillator prototype for IS-137 dual-mode standard has been implemented in a 0.35μm CMOS technology. A discussion of specific implementation details including complete circuit schematics and layout can be found in this chapter.

6.2 IS-137 Dual-Mode Standard

IS-137 [84], also known as the dual-mode TDMA/AMPS system, is a Time Division Multiple Access (TDMA) digital cellular standard that is backward compatible with the widely available Advanced Mobile Phone System (AMPS), commonly known as the "analog" cellular system.

The operating frequency range for IS-137 is between 824 - 849 *MHz* for the mobile transmit and 869 - 894 *MHz* for the mobile receive; and each channel occupies 30 *kHz* of bandwidth. The required RF sensitivity for all channels over which the mobile station is

designed to operate is -116 *dBm* or better. With the 50Ω source noise power spectral density (PSD) being -174 dBm, the available noise power at the input can be derived to be approximately -129 dBm.

$$-174dBm + 10 \cdot \log(30kHz) \cong -129dBm \qquad (6 - 1)$$

Assuming the required SNR (Signal-to-Noise Ratio) to achieve an acceptable BER (Bit Error Rate) is 5 dB, the system noise figure is then 8 dB.

$$-116dBm - (-129dBm + 5dB(SNR)) \; = \; 8dB(NF) \qquad (6 - 2)$$

With the fundamental RF sensitivity requirement described above, the information provided below only contains sections of the IS-137 standard that are relevant to the local oscillator design, in particular for the Mobile Station (MS). The key specifications are described in the *adjacent and alternate channel desensitization* and *intermodulation spurious response attenuation* sections.

The *adjacent/alternate channel selectivity and desensitization* of a receiver is a measure of its ability to receive a modulated input signal on its assigned channel frequency in the presence of a second modulated input frequency spaced either one/two channel (30/60 *kHz*) above or below the assigned channel. The *intermodulation spurious response attenuation* of the receiver is the measure of its ability to receive a modulated input RF signal frequency in the presence of two unmodulated interfering signals assigned at specific frequencies. The IS-137 standard has separate specifications for the analog and digital modes of operation.

Analog Mode Operation

The *adjacent/alternate channel selectivity and desensitization* is measured by connecting two RF signal generators to the receiver. Set one RF signal generator at reference sensitivity (-116 *dBm*) and increase by 3 *dB*. Set the frequency of the second RF signal generator to either 30/60 *kHz* above or below the first RF signal generator. Adjust the level of the second RF signal generator until the output SNR reduces back to 5 *dB*. Or equivalently, the adjacent/alternate channel interference generates an equal amount of noise as the system noise floor, hence reduce the SNR by 3 *dB*.

The minimum adjacent/alternate channel selectivity is 16 *dB* / 60 *dB*. To calculate the phase noise required for the adjacent channel

$$-16dB - 10 \cdot \log(30kHz) - 5dB(SNR) = -66dBc/Hz @ 30\ kHz \qquad (6\text{ - }3)$$

or equivalently, it can be calculated by measuring the adjacent/alternate channel power to the system noise floor. The adjacent channel power is $-116dBm + 16(dB) = -100dBm$ and the system noise floor is $-129dBm + 8dB(NF) = -121dBm$. The phase noise for the adjacent channel is

$$-121dBm - (-100dBm) - 10 \cdot \log(30kHz) = -66dBc/Hz @ 30\ kHz \qquad (6\text{ - }4)$$

Same method suggests the phase noise requirement for the alternate channel is $-110dBc/Hz$ @ 60 *kHz*.

A similar experiment is performed for the *intermodulation spurious response attenuation*. Instead of one RF signal generator as the interference signal, two RF signal genera-

tors are used. While the desired signal is set at 3 *dB* above the reference sensitivity, the levels of two RF interference signals are adjusted together until the output SNR falls back to 5 *dB*.

Two tests are performed for the intermodulation attenuation. The close-spaced intermodulation spurious response attenuation for a pair of signals at 60 *kHz* and 120 *kHz* is 65 *dB*. The wide-spaced intermodulation spurious response attenuation for a pair of signals at 330 *kHz* and 660 *kHz* is 70 *dB*. To calculate the phase noise required for the close-spaced case,

$$-65dB - 10 \cdot \log(30kHz) - 5dB(SNR) - 3dB = -118dBc/Hz @ 60\ kHz \qquad (6\text{-}5)$$

where the 3 *dB* is accounting for the contributions from both spurious tones. Similarly, $-123dBc/Hz$ @ 330 *kHz* is required for the wide-spaced intermodulation.

Digital Mode Operation

In digital mode operation, the *adjacent/alternate channel selectivity and desensitization* is identical to that of analog mode operation. For the *intermodulation spurious response attenuation*, only one test of two RF interferences are specified by the standard. The intermodulation spurious response attenuation for a pair of signals at 120 *kHz* and 240 *kHz* is 65 *dB*. This, in turn, translates to a phase noise of $-118dBc/Hz$ @ 120 *kHz*.

Table 6-1 summarizes the phase noise requirements for the IS-137 dual-mode standard. The shaded boxes indicate the critical phase noise specification for the design. For GSM family standard, the required phase noise at 600 *kHz* is -122 *dBc/Hz* [85]. Normaliz-

ing this value to 60 *kHz* using 20 *dB/dec* phase noise roll-off in a VCO, the equivalent phase noise required at 60 *kHz* is -102 *dBc/Hz*. Therefore, the IS-137 system has a much more difficult phase noise specification.

TABLE 6-1 Summary of Phase Noise Spec. for IS-137

Offset Frequency	Analog Mode	Digital Mode
30 kHz	-66 dBc/Hz	-66 dBc/Hz
60 kHz	-110 dBc/Hz	-110 dBc/Hz
60/120 kHz	-118 dBc/Hz	n/a
120/240 kHz	n/a	-118 dBc/Hz
330/660 kHz	-123 dBc/Hz	n/a

6.3 Technology

The experimental prototype was fabricated in *STMicroelectronics* HCMOS6 0.35μm 3.3V process. This process includes two layers of poly and five layers of metal. In addition, it also features passive devices such as poly-poly capacitors, diffusion resistor, varieties of controlled poly resistors and a high ohmic poly resistor. Due to the non-disclosure agreement (NDA) with *STMicroelectronics*, no further details can be released regarding the process at this time.

6.4 Chip Overview

Fig. 6.1 shows an implementation block diagram of the frequency-multiplier IC. A nine-stage delay chain with a 100 *MHz* input crystal oscillator is locked to the half-period of the reference frequency, and it generates edges triggered by the crystal oscillator transi-

tions to form the 900 MHz output. In many modern transceiver architectures (described in Chapter 2), I/Q quadrature signals are required. To generate signals that are quadrature in phase (90 degrees or $\pi/2$ out of phase), each delay stage consists of two delay cells of the type shown in Fig. 5.9. The additional delay cells generate new edges that are $\pi/2$ apart in the output waveform period and allow straightforward generation of a quadrature LO signal with an additional edge combiner. This is shown in Fig. 6.1. The required additional delay cells and buffers are included on the experimental chip but the additional edge combiner is not included. The buffers consist of three differential pairs cascaded to drive the edge combiner inputs.

Fig. 5.9 showed a detailed circuit schematics of a delay cell with the replica bias circuit. The nominal required delay per stage for this implementation is

$$\frac{1}{9 \cdot f_{ref}} \times \frac{1}{2 \times 2} = \frac{1}{9 \cdot 100MHz} \times \frac{1}{4} = 278ps \qquad (6 - 6)$$

The crystal oscillator input is first amplified by a differential amplifier to increase the signal level, then applied to the delay chain input. A replica bias circuit is used to adjust the load resistance in the delay cells for a fixed output voltage swing and proper time delay. Buffers, identical to the delay cell, are placed at the output of each delay cell not only to sharpen the transitions but also to present equal loading to each DLL output node. A separate replica bias circuit is used to adjust the load resistance of the buffer to ensure a fixed voltage swing for process variations. The output of the delay buffers are waveforms that are evenly spaced within the reference period and nearly a squared wave.

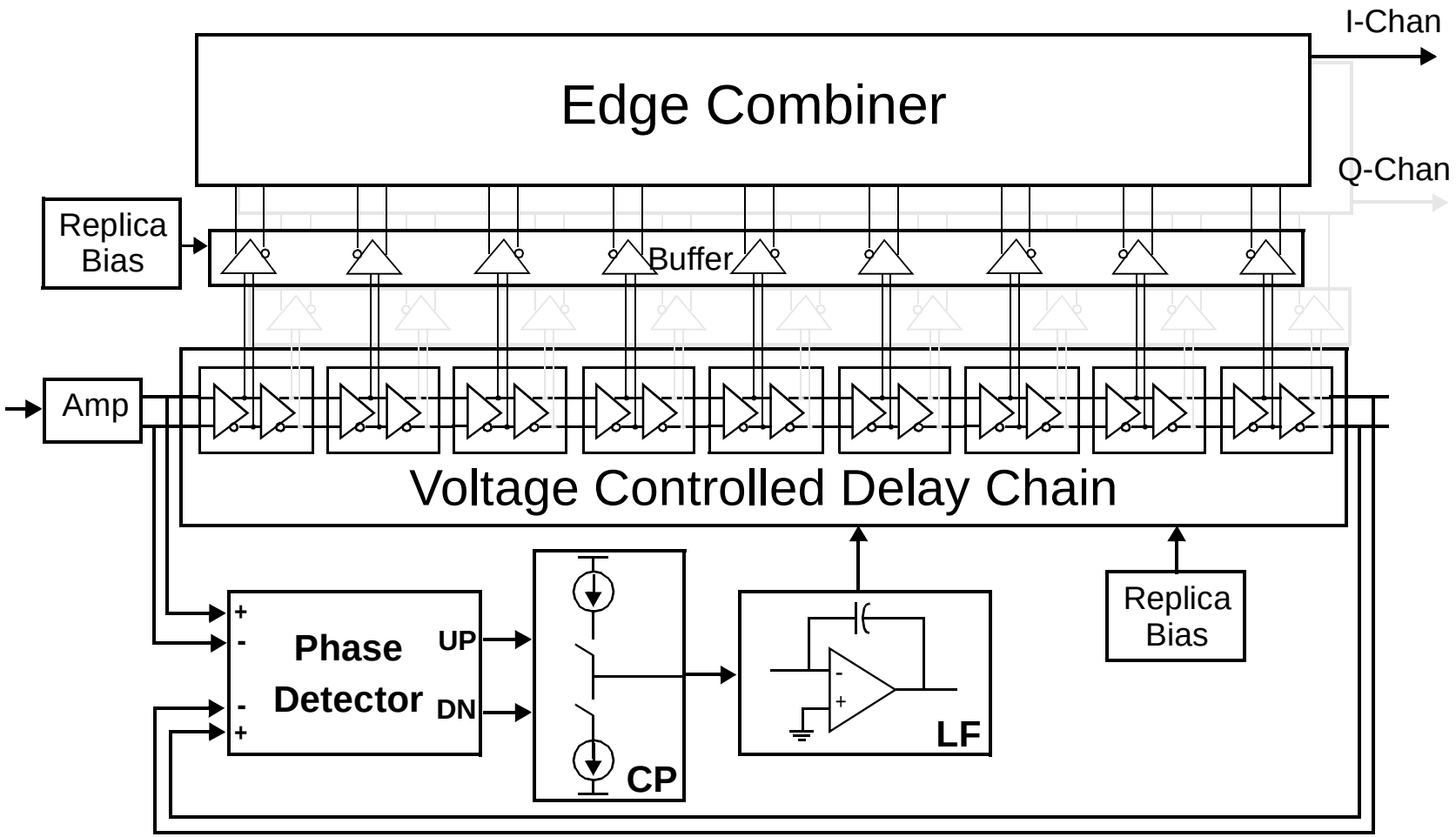

Fig. 6.1: Chip Implementation Block Diagram.

These waveforms are then used as inputs to the edge combiner to generate the desired output frequency.

In this prototype, an on-chip master bias circuit is used to generate a reference current that is mirrored throughout the entire chip to provide the biasing current.

6.5 Master Bias

Fig. 6.2 shows the circuit schematic of the master current bias used on chip. It utilizes a feedback loop to match the ΔV_{be} difference in a pair of *unmatched* bipolar devices to a $\Delta(V_{GS}-V_T)$ difference in a pair of *unmatched* MOS devices. Transistors Q1 and Q2 are a pair of *unmatched* bipolars whose area are 20X difference in size. M1 and M2 are source followers for level shifts. M3 and M4 also have the size mismatch. With feedback, the current is

$$I_{SS} = \frac{\mu C_{ox}}{2} \cdot \left(\frac{W}{L}\right)_3 \cdot \frac{\left[\frac{kT}{q} \cdot \ln(X)\right]^2}{\left[1 - \sqrt{\frac{(W/L)_3}{(W/L)_4}}\right]} \qquad (6\text{ - }7)$$

A start-up circuit, not shown in Fig. 6.2, is also included in this design. Similar bias circuits can be found in [86] or other analog IC reference books.

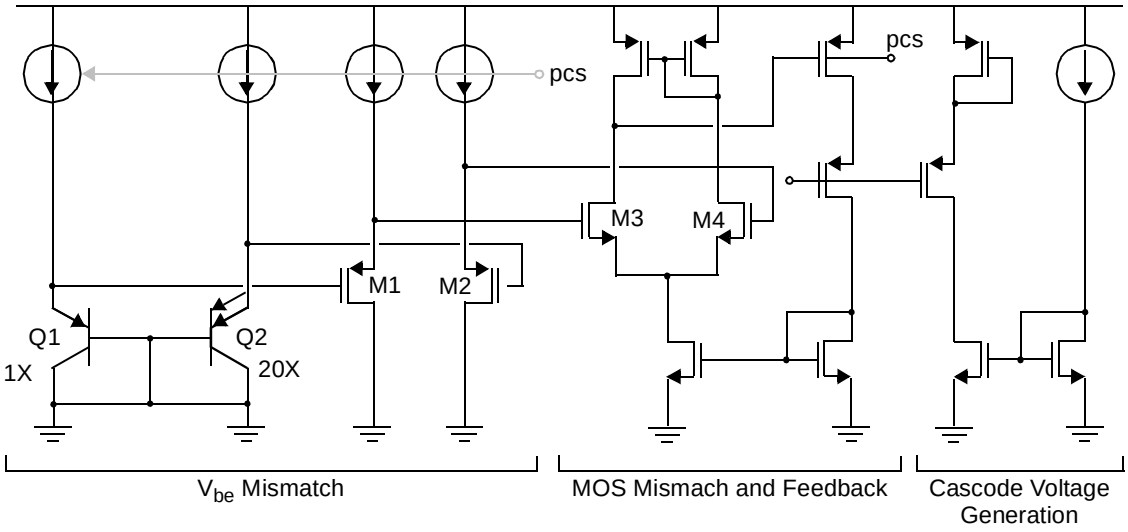

Fig. 6.2: Circuit Schematic for Master Bias.

6.6 Output Buffer

The outputs of the edge combiner are DC level-shifted down to approximately $V_{DD}/2$ and connected to a pair of open drain NMOS devices. The NMOS devices are loaded with 50Ω resistors externally through bondwires and connected to the measurement equipment.

6.7 Performance Estimation

Using the circuit parameters according to the design shown in the previous chapter, the phase noise performance can be estimated using the thermal-noise-induced random timing error for the delay cell [89][90][91] and the DLL random-timing-error correlation

analysis presented in Chapter 4. The normalized timing error of a differential delay cell shown in Fig. 5.9 can be described as

$$\frac{\Delta t_{d(rms)}}{t_d} = \sqrt{\frac{kT}{C_L}} \cdot \frac{1}{(V_{GS} - V_T)} \cdot \xi \qquad (6 - 8)$$

This analysis is summarized in Appendix A for completeness. Extra capacitance, $C_L \cong 100fF$, was added to each delay cell output to achieve the required delay. $V_{GS} - V_T$ of NMOS input devices is approximately 500 mV. The noise contribution factor ξ is approximately 1.5 for this circuit topology.

To estimate the phase noise of DLL frequency multiplier in terms of the normalized timing jitter, Eq. 4 - 16 (repeated here for clarity) is used.

$$S_T(\Omega) = \sum_{n=-\infty}^{\infty} \left\{ \frac{1}{N} \cdot \sum_{k=-(N-2)}^{N-2} \left[\delta(n-k) \cdot \sum_{l=1}^{N-|n|-1} l \cdot \sigma^2 \right] \right\} \cdot e^{-j\Omega n} \qquad (6 - 9)$$

where $N = 9$ is the number of stages, Ω is the normalized frequency and σ^2 is the variance of the timing jitter which is equal to $(\Delta t_{d(rms)})^2$. This equation describes an implementation of the DLL-based frequency multiplier shown in Chapter 4, however, does not consider the design specifics added for this actual prototype (i.e., I/Q generation and others described in Fig. 6.1).

Using Eq. 6 - 9 as a starting point, and taking into consideration the specific implementation details for this prototype, the phase noise equation can be simplified to,

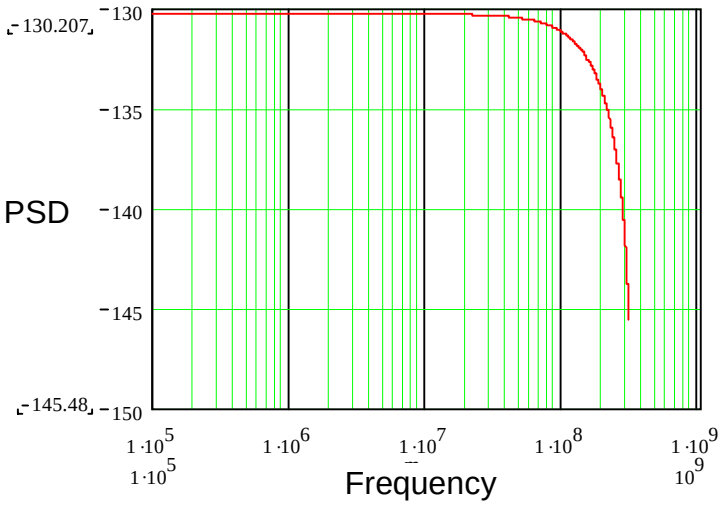

Fig. 6.3: Phase Noise Prediction.

$$S_T(\Omega) = \left(\frac{1}{9}\cdot\sigma^2\right)\times(126 + 142\cdot\cos\Omega + 110\cdot\cos 2\Omega + 102\cdot\cos 3\Omega + 118\cdot\cos 4\Omega$$

$$+ 102\cdot\cos 5\Omega + 78\cdot\cos 6\Omega + 62\cdot\cos 7\Omega) \qquad (6\text{ - }10)$$

for this example. Fig. 6.3 shows the phase noise prediction in a log-log plot. This also accounts for the random timing error added by the crystal buffer before the delay chain, buffers after the delay chain and the edge combiner. Since both buffer and edge combiner input devices used in this prototype are identical to the delay cell, it has been shown in [89] that these circuits contribute a white noise spectrum. The predicted phase noise agrees with the intuition where the noise profile is constant for frequencies within the reference frequency. The role of integrated spiral inductors in the edge combiner is only to enhance the LC-tank impedance at the resonance frequency (i.e., 900 *MHz*). Hence, the phase noise performance does not depend on the spiral inductor quality factor.

6.8 1/f Noise

The flicker or $1/f$ noise, caused by crystal defects on semiconductor substrate, is often problematic in integrated circuits. Fig. 2.15 shows that a typical VCO phase noise also has a $1/f$ noise component in its output spectrum.

In the DLL-based frequency multiplier shown in Fig. 6.1, $1/f$ noise is present in all circuits with active current sources, however, it is not detected at the output around the desired frequency. For example, the $1/f$ noise present in the current source of a delay cell is modulated by the input signal to f_{ref} (same situation for the buffer stages). $1/f$ noise present in the edge combiner current sources are also modulated up to f_{ref}. Since all these $1/f$ noise sources are independent from each other, when the currents are summed in the edge combiner, only the uncorrelated "white" noise is present at the output. In other words, $1/f$ noise is only modulated to the DLL reference frequency but not the output carrier frequency. This result also contributes to the low phase noise at the close-in frequency.

6.9 Layout

Fig. 6.4 shows the chip micrograph of the DLL-based frequency multiplier. Differential crystal inputs are brought in from the LHS and the differential RF outputs are taken from the bottom. The input and output pads are oriented at a 90° angle to minimize the mutual inductance coupling between bondwires. The delay chain is placed horizontally in

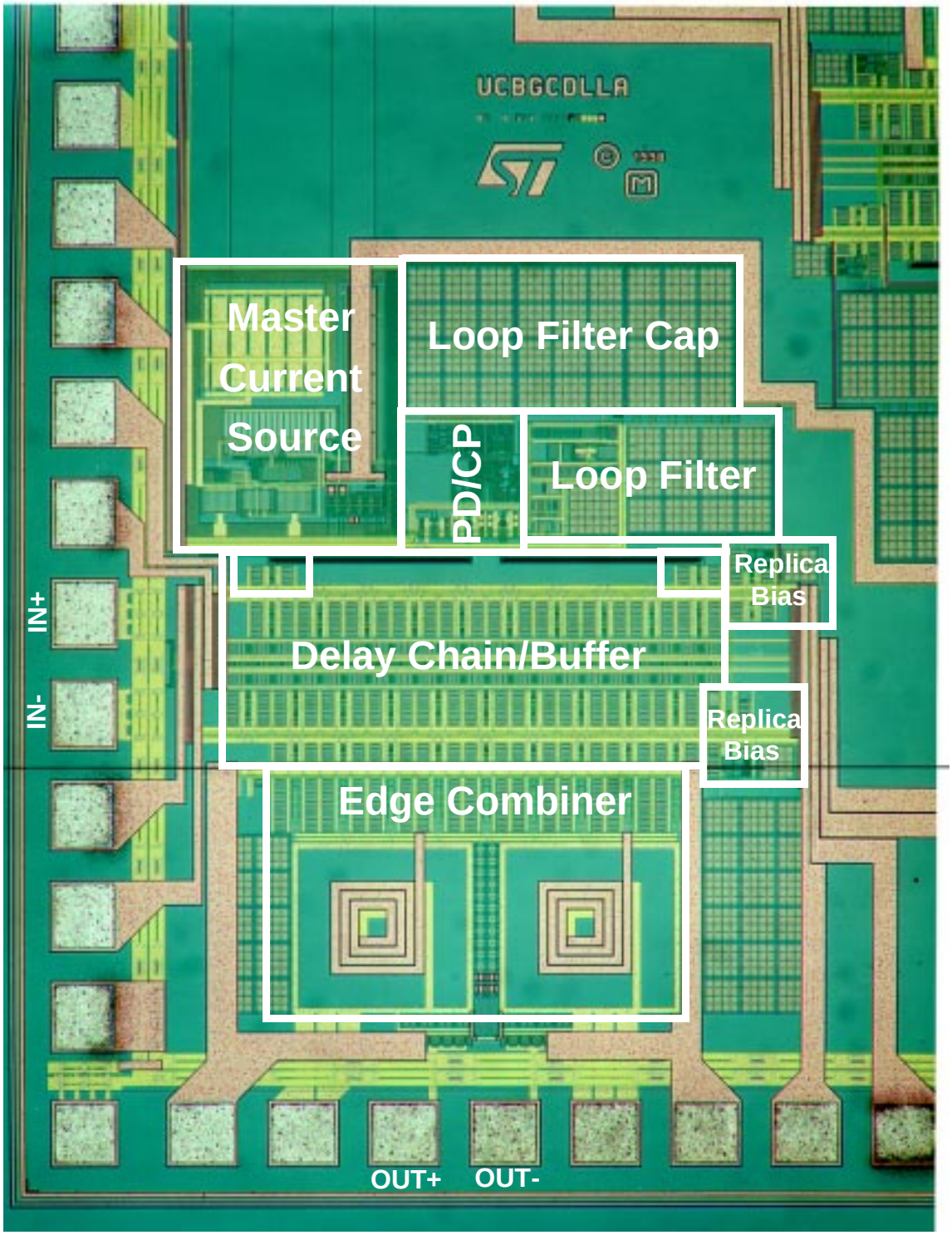

Fig. 6.4: Die Micrograph.

the center with buffers driving the edge combiner just below the delay chain. The input and output of the delay chain (indicated in small boxes at upper right and left corners of delay chain) are used as inputs to the phase detector. Through the charge pump and loop filter, the circuit generates a control voltage to achieve the desired locking condition. A master current source with large lateral PNP devices can be found at the upper left corner. Two replica bias circuits are located next to the delay chain and delay buffers for the respective circuit blocks.

With the ultimate goal of this research being a fully integrated transceiver, the design pays special attention to noise immunity since some of the other functional blocks in a radio transceiver are potential noise generators, i.e., A/D converters, switched-capacitor filters, etc. The differential circuit topology is used throughout the design and multiple substrate taps are placed close to the noise sensitive circuits to avoid the noise injection. For analog blocks, substrate taps are placed close to the NMOS transistors and connected to an analog GND nearby (for common-source configuration, substrate taps are connected to the source, commonly known as *budding contact*). For digital blocks, substrate taps are placed close to NMOS transistors and connected to a separate SUB pin to a dedicated output pad. This pad is then joined with GND on the evaluation board. An added advantage for placing substrate taps close or next to transistors is to minimize the body effect variation. For common-source devices, no body effect is found since the source and body are connected. For cascode devices, although the source potential may vary with respect to the body potential, the effect of V_T on the drain current is greatly reduced due to the source

degeneration. No additional substrate taps are placed with fears that they may act as noise receptors to couple extra noise into the circuit [92].

Separate V_{DD} and GND pins are used for each functional blocks not only to minimize the noise coupling between different circuit blocks, but also to reduce the overall impedance to ground. Multiple V_{DD} and GND are used throughout the chip. The digital V_{DD} and GND are separated from the analog ones. Within the analog section, V_{DD} and GND for different functional blocks are also separated to have more flexibility in terms of supply voltage variation, power measurement during the experiment.

The starting material for this process is the bulk p+ wafer with a thin epitaxial layer. This is done primarily to avoid the latch-up condition in digital circuits. However, this provides a low impedance path for noise generating circuits to couple noise. Because the noise signal stays in the low-resistive p+ region, the traditional isolation using grounded n-well guard rings to collect noise is not effective [92][93]. In this prototype, the die is attached to the circuit board directly with a conductive epoxy (this will be described in Chapter 7). The idea is to use the combination of the low impedance substrate and conductive epoxy to provide the lowest impedance path to GND for noise to travel.

Two large spiral inductors are visible in the die micrograph. Since the quality factor of the inductors does not affect the phase noise performance, the optimization performed with ASITIC [94][95][96] is to achieve the highest $Q^2 \cdot R_{eq}$ product for the maximum output swing. The two spiral inductors are laid out in the same orientation to minimize the

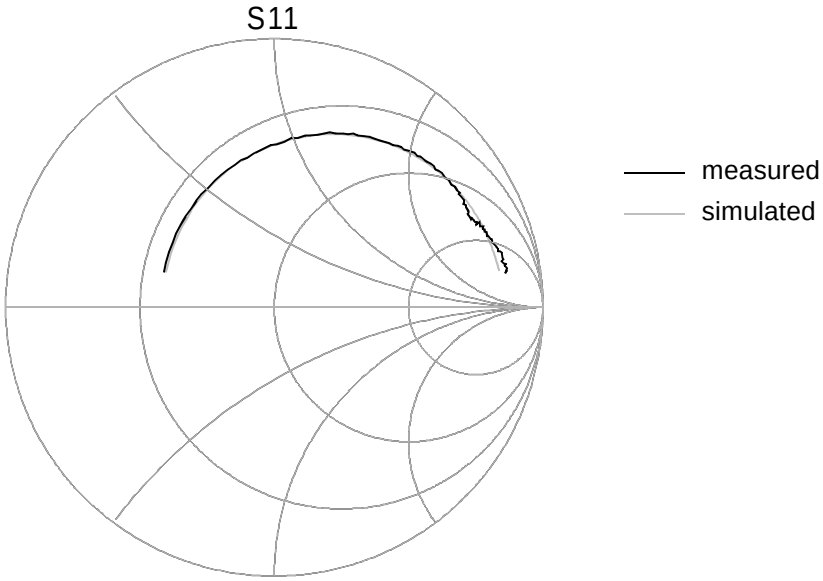

Fig. 6.5: S11 for Spiral Inductors.

mutual inductance because the output signals are differential. A separate test chip for the spiral inductor was fabricated in the same process. The simulated and measured values for the inductor are summarized in Table 6-2. Fig. 6.5 shows the measured S_{11} of the spiral inductor versus the simulated result.

TABLE 6-2 Spiral Inductor Summary

Spiral Inductor Model	Simulated	Measured
L	18.022nH	17.69nH
RS	17.810	20.5
Q @ 1GHz	4.9	5.4

6.10 Summary

The DLL-based frequency multiplier has been implemented and fabricated using STMicroelectronics 0.35μm CMOS process. Details about the IC have been described in

this chapter with the chip micrograph. Experimental data will be presented in the next chapter.

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Chapter 7

Experimental Results

7.1 Introduction

Following the design and fabrication of the experimental prototype, the DLL-based frequency multiplier has been characterized for its performance. The key performance measures for a local oscillator are its *phase noise* and *spurious tone* output. In this chapter, a detailed description of the test setup is provided in the next section. The performance data for phase noise and spurious tone are presented in Sections 7.3 and 7.4. A summary of relevant information about this integrated circuit can be found in Section 7.5.

7.2 Test Setup

The integrated circuit is packaged with the chip-on-board technology. With this technology, the bare die is directly attached to the circuit board with some conductive epoxy (for thermal and electrical conductivity) and bondwires are placed between the bonding pads on the chip and the gold-plated bondwire landing areas found on the circuit board. The gold plating is necessary for the bondwire to properly adhere to the landing area.

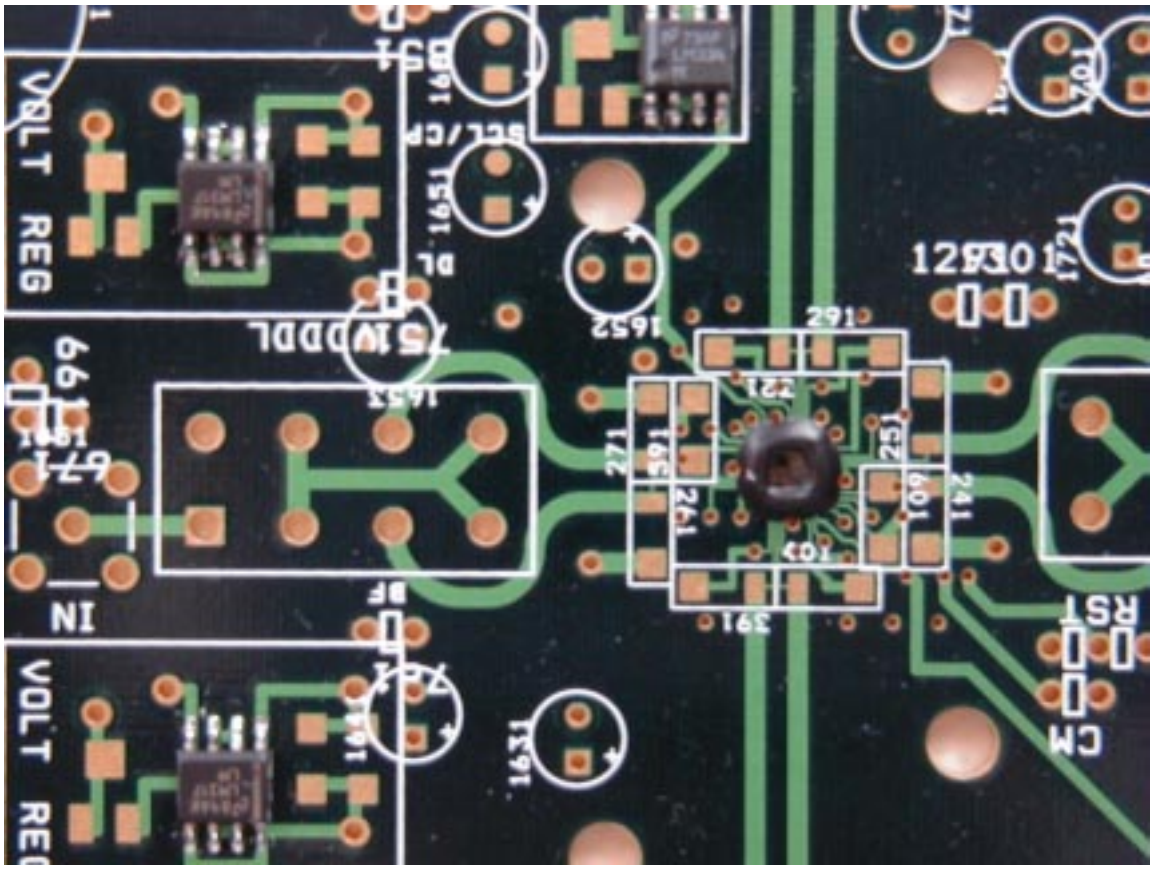

Fig. 7.1: Photograph of Chip-On-Board Area.

These bondwire landing areas on the board are designed to match the pitch on the IC to avoid angled bondwires. Fig. 7.1 is a close-up photograph of the die attach area on the test board. The die is located in the center right of the photo and the black epoxy is used on the edge of the die to protect the bondwires. Directly under the die (not shown) is a gold-plated die-attach area which is shorted to GND. This allows a direct connection between the Si substrate and the board GND, and a single GND is used on the test board to minimize the impedance. The 4-layer test board was constructed with the standard FR4 material. The top layer is mainly used for signal routing where as the bottom layer is used for control lines. The inner 'plane' layer that is 20 *mils* below the TOP layer is the com-

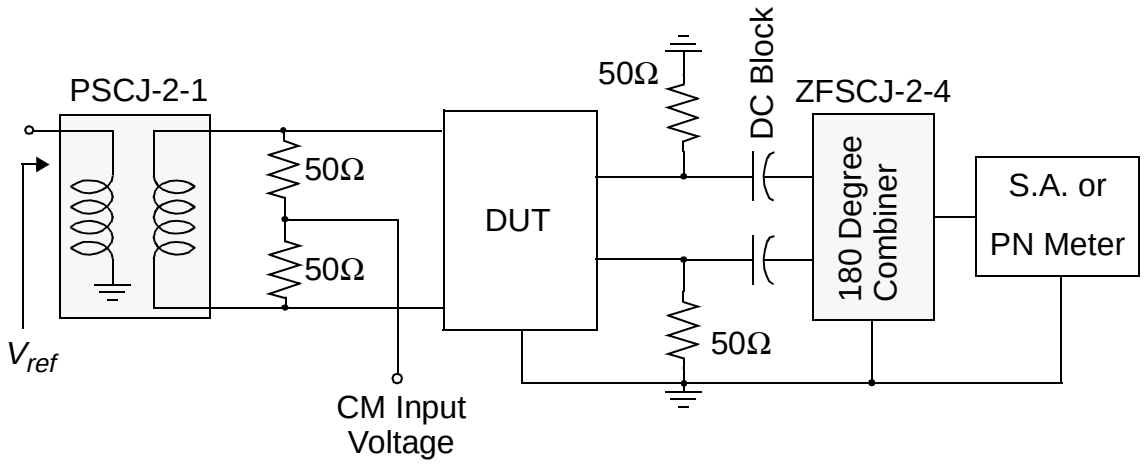

Fig. 7.2: Test Setup.

mon board GND, and it also provides the GND reference for the RF signal lines. The other inner 'plane' layer is the supply layer, and it is broken into several V_{DD} power planes to minimize the noise coupling as described in Chapter 6.

The basic test setup for this experiment is shown in Fig. 7.2. Each supply pin is connected to a National Semiconductor LM317 voltage regulator [97] whose configuration is shown in Fig. 7.3. Each regulator can be adjusted independently from others and the output voltage can be described as

$$V_{out} = 1.25 \cdot \left(1 + \frac{R_2}{R_1}\right) + I_{adj} \cdot R_2 \qquad (7 - 1)$$

Each supply pin is also bypassed to GND with a 10μF Tantalum capacitor and a 0.1μF Ceramic chip capacitor. In addition to the on-chip master current source described in Chapter 6, an optional external current source which is implemented with a National

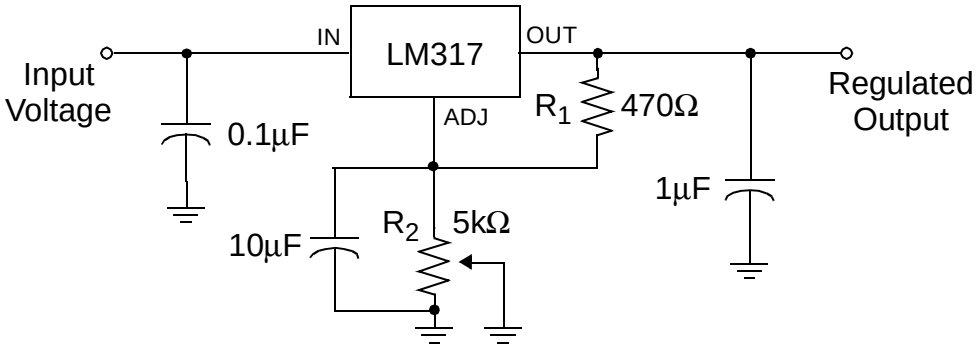

Fig. 7.3: Voltage Regulator Configuration.

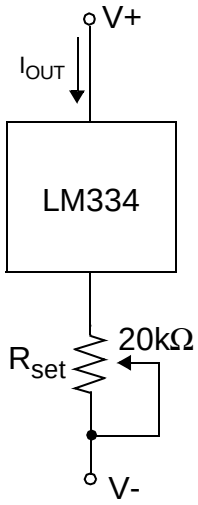

Fig. 7.4: External Current Source Configuration.

Semiconductor LM334 current source [98] can be used. The current source configuration is shown in Fig. 7.4 and its current level is set by adjusting R_{set} according to the following equation,

$$I_{out} \approx \frac{227\mu V/KT}{R_{set}} = \frac{68mV}{R_{set}} \qquad (7 - 2)$$

For the experiment, the 100 *MHz* sinusoidal reference frequency, V_{REF}, is generated by either a customized Vectron crystal oscillator (233FW-RL2) or a Rhode-Schwartz RF signal generator (SME03). This signal comes on-board through a SMA connector and is applied to a transformer (Mini-Circuit PSCJ-2-1) which converts the single-ended signal to a balanced, differential signal. These components are also shown in Fig. 7.1. The outputs of the transformer are DC level-shifted to a common-mode input voltage and terminated with two 50Ω matching resistors. The common-mode input voltage can be adjusted with a voltage regulator and is nominally set at 2.8V.

The balanced, differential outputs of the IC are loaded with two 50Ω matching resistors and passed through two DC blocking caps. The DC blocking caps are used to remove the DC content of the output signals to protect the spectrum analyzer. A 180-degree RF combiner (Mini-Circuit ZFSCJ-2-4) is used to combine the different outputs into a single-ended output. This single-ended output waveform is measured with HP8563E Spectrum Analyzer and HP3048A Phase Noise Measurement System for its performance.

7.3 Phase Noise Performance

Different modern RF equipment can be used to measure the single-sideband phase noise of a frequency synthesizer. Some are dedicated phase noise measurement systems, while others are general purpose Spectrum Analyzers with the built-in phase noise function. In general, a spectrum analyzer with the phase noise measurement capability (such as the HP8563E series Spectrum Analyzer) offers a smaller dynamic range, hence, the phase

noise floor is limited. Other systems that are dedicated to measure the frequency synthesizer performance (such as HP3048A, HP4352S VCO/PLL Test System, or RDL systems) usually have a much lower noise floor.

The following measurement results are collected from a HP3048A phase noise measurement system provided by National Semiconductor-Wireless Communication Group. The measurement system is set up inside a Faraday cage which blocks virtually all RF signals that are present in the ambient environment.

The measured single-sideband phase noise plot is shown in Fig. 7.5 with IS-137 requirements superimposed on the plot. Due to equipment limitation, only offset frequencies in the range of 10 *kHz* to 40 *MHz* can be measured. The phase noise profile agrees with the analysis in Chapter 5 where the phase noise floor is roughly constant within the reference frequency. The small increase in phase noise for low offset frequency may be due to the $1/f$ noise of the open-drain output buffer devices described in Chapter 6. The measured phase noise in the constant region is approximately -127 *dBc/Hz*.

For a carrier frequency of 900 *MHz*, the single-sideband phase noises of -120, -123 and -127 *dBc/Hz* at 30, 60, and 330 *kHz* offset frequencies are measured. These offset frequencies are the critical ones that satisfy the IS-137 specification as summarized in Table 6-1.

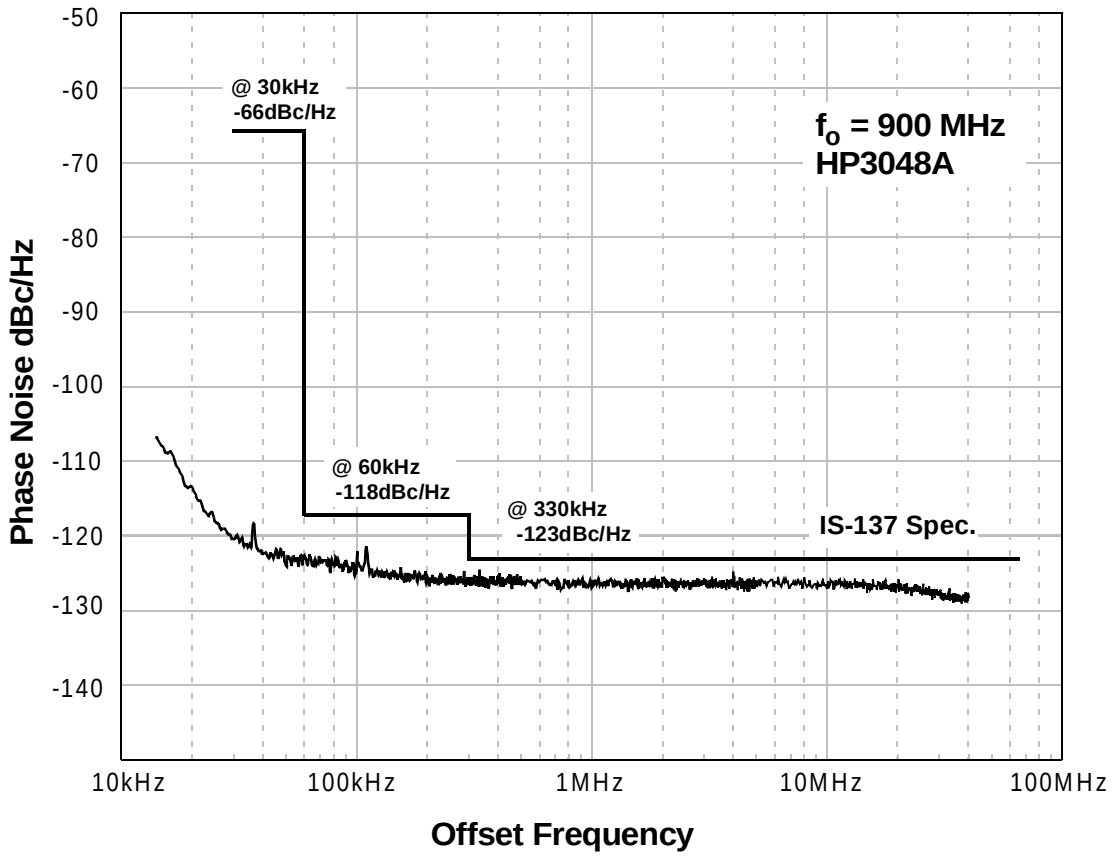

Fig. 7.5: Single Sideband Phase Noise Plot with IS-137 Requirements.

7.4 Spurious Tone Performance

The spurious tone measurement was performed by using the general purpose HP8563E Spectrum Analyzer and sweeping through the frequency range around the carrier frequency. Fig. 7.6 shows the spectral plot of the local oscillator output. The center frequency is at 900 MHz. Within a frequency span of 160 MHz, no observable spurious tones are present. The nearest spurious tones appear at 100 MHz away from the center frequency (800 MHz or 1 GHz). Fig. 7.7 shows a 250-*MHz* span spectral plot of the

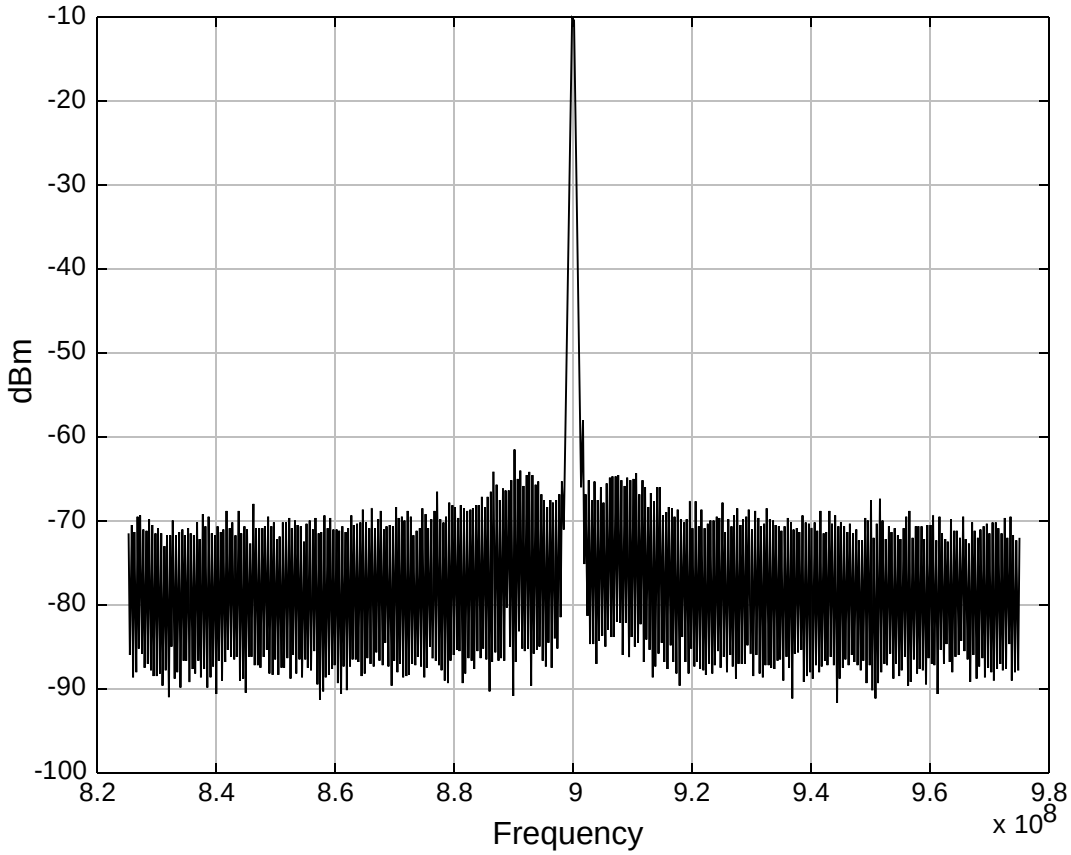

Fig. 7.6: Output Spectrum Plot.

LO output signal in the upper sideband. The spurious tones are found at 1 and 1.1 *GHz* which are at integer multiples of 100 *MHz* away from the center frequency. The lower sideband exhibits a very similar graph.

Although the nearest spurious tone of -30 dBc is measured, the location being 100 *MHz* away from the center frequency makes the spurious tone's effect on RF systems minimal. In a typical RF transceiver system, the front-end RF filter attenuates signals that are outside of the received RF bandwidth. In the case of IS-137, the RF bandwidth is only 25

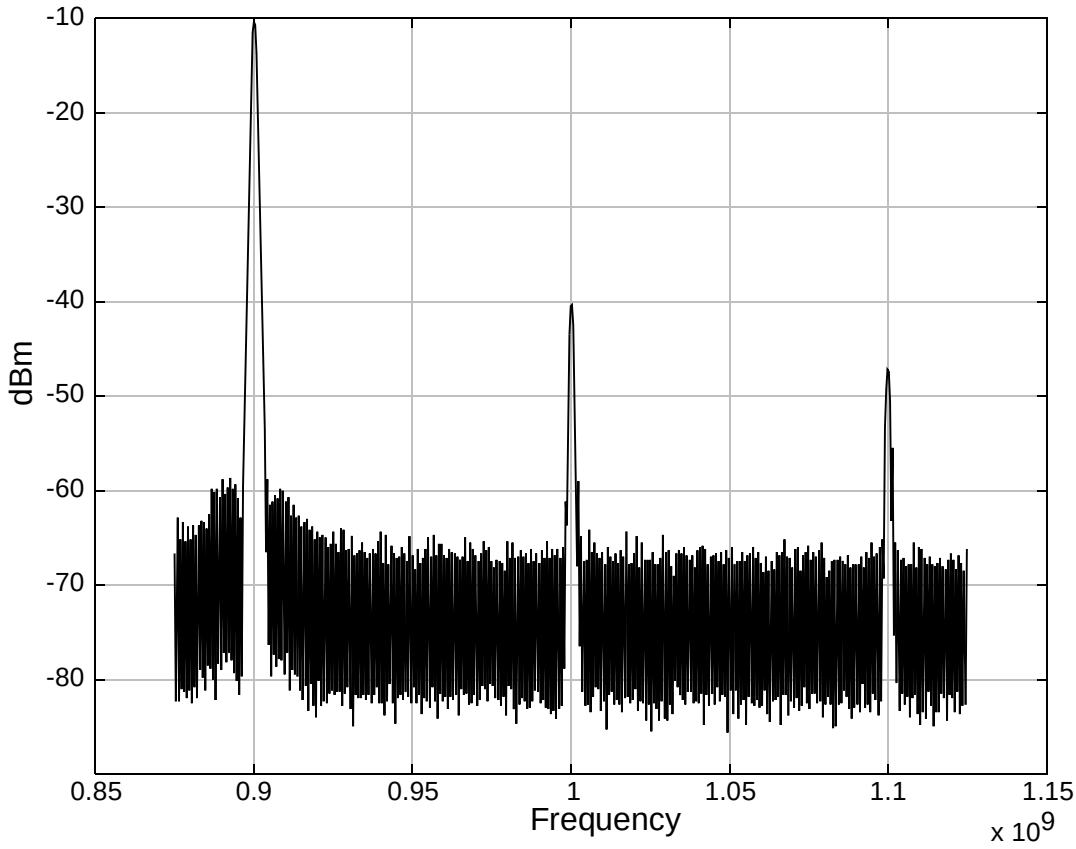

Fig. 7.7: Spurious Tone Plot.

MHz for transmit or receive. Therefore, outside the 25 *MHz* band, the signals are attenuated substantially.

7.5 Summary

Measurements were performed across five different samples and they all exhibit very similar performance as presented above. Table 7-1 summarizes the measured results along with other related information.

TABLE 7-1 Summary of the Prototype Characteristics

V_{DD}	3.3V
Technology CMOS	0.35μm CMOS
Output Frequency	900 MHz
Output Level	-10 dBm
Phase Noise	-120 dBc/Hz @ 30kHz -123 dBc/Hz @ 60kHz -127 dBc/Hz @ 330kHz
Spurious Tones	-30dBc @ 100MHz o/s -37dBc @ 200MHz o/s
Power Consumption	130mW
Active Area	1.2 x 1.0 mm^2

The power consumption by blocks is summarized in the Table 7-2. The majority of power is consumed in the buffers which are placed at each DLL output to ensure equal loading (including both I/Q delay cells). These buffer stages are identical to the delay cell shown in Fig. 5.9 without the extra capacitors. To keep the random timing error low in the same order of magnitude, the power consumed by these buffers are comparable to the delay cells. Non-optimal charge pump and loop filter designs in this prototype also consume approximately 10% of the total current.

TABLE 7-2 Power Consumption by Blocks

Block Name	Current Consumption
Delay Chain	8.8mA
Buffer Cells	20.5mA
Edge Combiner	7.8mA
Phase Detector	0.6mA
Charge Pump/Loop Filter	1.8mA
Total	39.4mA

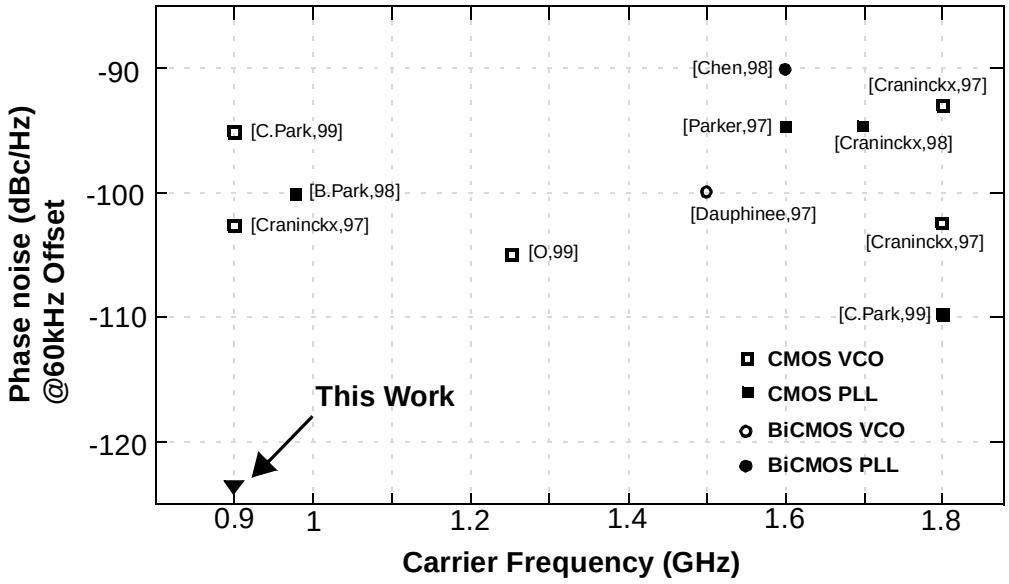

Fig. 7.8: Comparison of Recently Published Integrated VCO/PLLs.

One of the major advantages for the DLL-based frequency multiplier is that the required additional hardware (delay cells and buffers) to generate the I and Q signals are included on this prototype (shown in Fig. 6.1). With an additional edge combiner, the quadrature local oscillator signal can be generated with a straightforward fashion and a small power penalty (about 15%). In the case of a conventional PLL where quadrature signals are not available, various circuits (either active or passive) are required to generate the I/Q signals, which may consume as much power as the PLL itself.

Fig. 7.8 shows a comparison of phase noise at 60kHz offset frequency from recently published integrated VCO/PLLs. This work demonstrates a method to generate a local oscillator signal with a very low phase noise at a low offset frequency. The list of publications is included in the *Reference* [99] - [108].

7.6 References

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Chapter 8

Conclusion

8.1 Conclusion

It is clear that the growth in demand for wireless voice and data communications has driven recent efforts to substantially increase the integration level of RF transceivers for cost and form-factor reasons. One approach is to implement all the RF functions in the low-cost CMOS technology, so that the RF and baseband sections can be combined in a single chip. This in turn dictates an integrated CMOS implementation of the synthesizer and local oscillator functions with the requisite phase noise performance.

The conventional approach for the local oscillator design using a PLL requires large loop filter capacitors and does not suppress the poor phase noise performance of a monolithic VCO. The new transceiver architecture with a fixed-frequency LO_1 allows new explorations of integrated low-phase-noise local oscillator design. This method has been demonstrated using a wide loop bandwidth PLL example for a DCS1800 application. However, for RF systems such as AMPS where the channel spacing is small and close-in phase noise is extremely low, the wide loop bandwidth PLL does not provide enough sup-

pression for the poor VCO phase noise that is mainly due to the low quality factor of the on-chip spiral inductors.

The dissertation proposes a new concept using the DLL-based frequency multiplier that offers a limited random timing error accumulation in the delay chain. This unique accumulation pattern consequently achieves an excellent long-term jitter performance that is equivalent to low close-in phase noise. The thesis also explores the fundamental performance limits of the proposed concept based on the thermal-noise-induced timing jitter of delay cells in the DLL. The analysis suggests a constant phase noise profile for offset frequencies less than f_{ref}, and this agrees with both the intuition and the experimental result. The result demonstrates that the DLL-based frequency multiplier approach in deed provides a monolithic solution for a LO design whose phase noise is independent of the low-Q on-chip component and satisfies the stringent requirements of AMPS.

The specific research contributions of this work include (1) proposing a new local oscillator architecture using a DLL-based frequency multiplier that breaks the traditional LO phase noise limitations, (2) an analytical model that describes the phase noise performance of the proposed local oscillator architecture, (3) application of the DLL-based frequency multiplier to a monolithic CMOS low-phase-noise local oscillator for cellular phone applications. In particular, the experimental prototype generates a 900-MHz carrier and is implemented in a 0.35μm CMOS technology. It achieves -123 dBc/Hz phase noise at 60kHz offset while dissipating 130mW from a 3.3V supply. This approach demonstrates a fully-integrated CMOS local oscillator that satisfies the IS-137 standard.

Practical power-dissipation levels required for applications of this type are in the range of 25-75mW. This experimental prototype contains several design choices to facilitate testability and flexibility. Significant amount of the power is dissipated in these redundant blocks which can be eliminated. It is projected that a fully-optimized synthesizer producing both I and Q outputs at 900MHz using this architecture would dissipate about 110mW in 0.35μm technology and 80mW in 0.25μm technology, including mixer drive power. While this dissipation is higher than what would be achieved with an external high-Q varactor-tuned approach, the technique provides an attractive alternative where form factor and maximum integration level are of critical importance.

An interesting continuation of this work would be to dramatically reduce the power consumption with a minor modification on the DLL architecture. One possible solution is to make the current one-pass delay chain into a re-circulating one. In the re-circulating delay chain, the amount of delay stage and buffer hardware required is greatly reduced, therefore the static power dissipation is substantially decreased as well. Furthermore, it still maintains the same timing jitter accumulation pattern as the one-pass delay chain by taking advantage of each relatively jitter-free edge coming from the crystal oscillator. Since the delay stage and buffer dissipate well over 50% of power consumed in this current design, the new re-circulating delay chain method can potentially reduce the power by a factor two to three.

Appendix A

RMS Timing Jitter for Differential Delay Cell

A.1 Introduction

In this appendix, a closed-form equation for the *r.m.s.* random timing error of the differential delay cell used in the phase noise performance analysis (Chapter 4) will be derived. The delay cell circuit schematic was shown in Fig. 5.9 and is repeated in Fig. A.1. This closed-form equation for the *r.m.s.* timing jitter of one delay cell is a function of the circuit parameters. This appendix includes an abridged version of the *r.m.s.* timing error analysis. Detailed derivations can be found in the references [109][110][111].

A.2 RMS Timing Jitter Analysis

Fig. A.1 shows the differential delay cell with thermal noise sources associated with each active transistor. Each delay cell is assumed to have a nominal time delay, t_d, and a

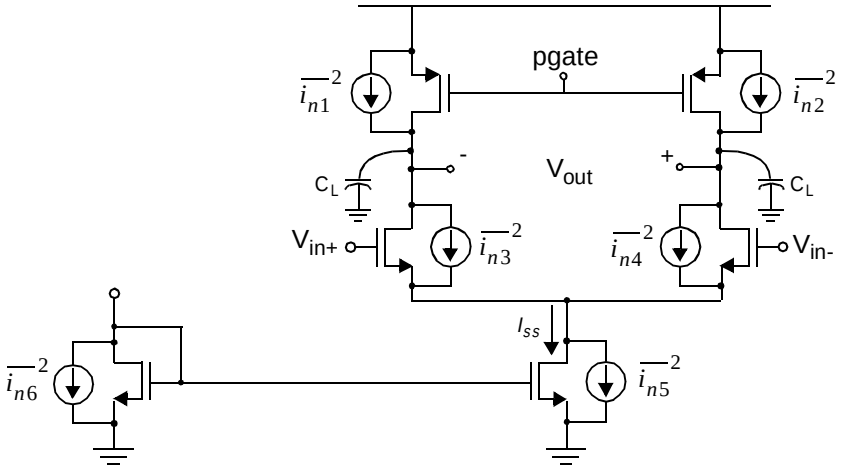


Fig. A.1: Differential Delay Stage with Thermal-Noise Sources.

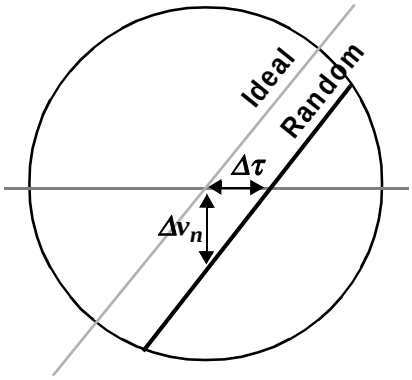
random timing error, $\Delta\tau$. The random timing error has zero mean and variance σ_t^2. In a simplified analysis, the nominal delay, t_d, is modeled as

$$t_d \cong V_{sw} \cdot \left(\frac{C_L}{I_{SS}}\right), \tag{A - 1}$$

where V_{sw} and C_L are the voltage swing and output load capacitance respectively, and I_{SS} is the tail current.

In this analysis, the random timing error can be estimated using the first crossing approximation, shown in Fig. A.2. Since the slope of the output transition (assumed linear) is I_{SS}/C_L, the voltage noise present at the output causes a random timing error which can be described with the following relationship,

$$\overline{\Delta\tau}^2 \cong \overline{\Delta v_n}^2 \times \left(\frac{C_L}{I_{ss}}\right)^2. \tag{A - 2}$$



$$\overline{\Delta\tau}^2 = \frac{\overline{\Delta v_n}^2}{(SlewRate)^2}$$

Fig. A.2: Differential Delay Cell with PMOS Triode Load.

Combining this with Eq. A - 1, we find the *normalized* timing error (the random timing error normalized to the time delay)

$$\frac{\overline{\Delta\tau}^2}{t_d^2} = \overline{\Delta v_n}^2 \cdot \left(\frac{C_L}{I_{ss}}\right)^2 \cdot \left(\frac{I_{ss}}{C_L V_{sw}}\right)^2 . \qquad \text{(A - 3)}$$

The voltage noise variance, $\overline{\Delta v_n}^2$, in Eq. A - 2 and Eq. A - 3 is the sum of thermal-noise contributions from each transistor in Fig. A.1. Although the variance of these noise sources depends on the state of the circuit, in this simplified analysis, they are assumed to have the values they would have with the circuit in the balanced state. By using the traditional noise model found in [112] and integrating the noise spectral density over the bandwidth of the lowpass filter formed by the load resistors and capacitors, we can write the *r.m.s.* random timing error for one stage, normalized to the time delay per stage, as

$$\frac{\Delta\tau}{t_d} \cong \frac{\Delta v_{rms}}{V_{sw}} = \sqrt{\frac{2kT}{C_L}} \cdot \left(\sqrt{1 + \frac{2}{3} \cdot a_v}\right) \cdot \frac{1}{V_{sw}} . \qquad \text{(A - 4)}$$

The normalized timing error is approximately equal to the voltage noise variance divided by the signal swing (from Eq. A - 1 and Eq. A - 2). The voltage noise has the familiar kT/C_L dependence and is a function of another modeling parameter called the noise contribution factor, ξ. In this case, $\xi = \sqrt{1 + \frac{2}{3}a_v}$ where a_v is the small-signal AC gain of the delay stage.

The next level of complexity in analysis drops the assumption that the variance of the noise sources is constant. Instead, one models the variance of the noise sources depend on the mode of circuit operation: (I) balanced mode (when the output is switching between two states, and transistors are all in linear or saturation region) (II) unbalanced mode (when the output has reached a state, and some transistors are in cut-off mode). For example, the tail current noise at the output is zero in the “balanced” mode (the noise is common-mode) and constant in the “unbalanced” mode. For NMOS input devices, the opposite is true. For PMOS triode devices, the noise at the output is nearly the same whether the system is in a balanced or unbalanced state. With these assumptions, the new noise contribution factor is,

$$\xi = \sqrt{1 + \frac{2}{3}a_v(1 - e^{-t/\tau}) + \frac{2\sqrt{2}}{3}a_v e^{-t/\tau}}, \qquad \text{(A - 5)}$$

where the time constant, τ, is approximately equal to the time delay of the stage. The second term rises exponentially to its equilibrium value as previously considered (Eq. A - 4) and the third term, due to the tail current noise, decays exponentially towards zero.

The next level of complexity in analysis incorporates the effects of adjacent stages and interstage amplification. Since the transition does not happen instantaneously, it is possible that more than one delay stage can be active at the same time. Therefore, a better model is to consider two successive stages and also consider the amplification of the noise voltage from the previous stage. The resulting noise contribution factor, ξ, for this model is higher by a factor of $(1/2)(a_v^2)$. With some re-arrangement, the new normalized random timing error expression can be shown to be

$$\frac{\Delta\tau}{t_d} = \sqrt{\frac{kT}{C_L}} \cdot \frac{1}{(V_{GS} - V_T)} \cdot \xi, \qquad \text{(A - 6)}$$

or the *r.m.s.* random timing error is given by

$$\Delta\tau = \sqrt{kTC_L} \cdot \frac{a_v}{I_{ss}} \cdot \xi. \qquad \text{(A - 7)}$$

This means the normalized *r.m.s.* timing error is the ratio of kT/C noise level to the gate voltage overdrive.

A.3 Implications

Eq. A - 6 shows that the normalized random timing error is equal to the ratio between the familiar kT/C_L noise power and the $V_{GS} - V_T$ bias point for the differential input transistors. The noise contribution factor, ξ, is relatively constant for this design.

The trade-off in choosing $V_{GS}-V_T$ is constrained by the voltage swing and interstage gain (shown in Chapter 5). To minimize $\overline{\Delta\tau}^2$ at a fixed swing, the $V_{GS}-V_T$ bias point should be maximized subject to the constraint that the interstage gain is more than one. For the kT/C_L trade-off, in order to make a useful comparison, some assumptions have to be made. The time delay, t_d, has to be kept constant for different cases by adjusting the circuit parameters. In this case, increasing C_L decreases the normalized random timing error as the square root rate at the expense of increasing power consumption and circuit area. The noise contribution factor, ξ, is affected by the interstage gain, a_v. Since a_v is constrained by V_{sw}, $V_{GS}-V_T$ and noise amplification, it cannot be manipulated much to improve ξ.

This is an abridged version of the analysis, please refer to the references below for details.

A.4 References

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Appendix B

Autocorrelation and Power Spectra

B.1 Introduction

The purpose of this Appendix is to provide some background information on the random process theory which was used in the phase noise analysis in Chapter 4. A more comprehensive discussion on this subject can be found in [113][114][115][116][117] or most technical books on random process.

B.2 Theory

Assume $X(t)$ is a random process. For any particular time instant t_0, $X(t_0)$ is a random variable. The first moment of the random variable (also known as its expected value) is defined as

$$m_{X(t_0)} = E[X(t_0)] = \int_{-\infty}^{\infty} u \cdot P_{X(t_0)}(u)du, \qquad \text{(B - 1)}$$

where $P_{X(t_0)}(u)$ is the probability density function (PDF). If the random process, $X(t)$, is stationary, this PDF does not change as a function of time. The first moment thus does not depend on t:

$$E[X(t_0)] = E[X(t_1)] = m_X, \quad \forall t_0, t_1. \tag{B - 2}$$

For $X_1 = X(t_1)$ and $X_2 = X(t_2)$, define

$$R_{XX}(t_1, t_2) \equiv E[X_1 \cdot X_2] = \int_{-\infty}^{\infty}\int_{-\infty}^{\infty} u_1 \cdot u_2 \cdot P_{X_1X_2}(u_1, u_2)du_1du_2, \tag{B - 3}$$

where $P_{X_1X_2}(u_1, u_2)$ is the joint probability density function of X_1 and X_2. The function $R_{XX}(t_1, t_2)$ is called the *autocorrelation* function of the random process $X(\boldsymbol{t})$, evaluated at $\boldsymbol{t} = (t_1, t_2)$. If the random process, $X(t)$, is stationary, the second joint moment is independent of the absolute time reference, and depends only on the difference between t_1 and t_2. In this case, Eq. B - 3 can be re-written

$$R_{XX}(t_1, t_2) = R_{XX}(t_2 - t_1), \qquad X(t) \text{ stationary.} \tag{B - 4}$$

Let $\tau = t_2 - t_1$, or $t_2 = t_1 + \tau$. Eq. B - 4 can then be further simplified to

$$R_{XX}(\tau) = E[X(t)X(t + \tau)], \qquad X(t) \text{ stationary.} \tag{B - 5}$$

Eq. B - 5 is the more familiar form of the *autocorrelation* function. A weaker definition for stationarity is a *wide-sense stationary* random process, in which the only restriction is that the *autocorrelation* depends only on time difference, τ. In the Gaussian distribution model used in the analysis, the two conditions are equivalent. The *autocorrelation* function mea-

sures how "similar" a particular value of a sample function is with another value that is τ units of time away.

If one can choose τ such that X_t and $X_{t+\tau}$ are practically independent, the autocorrelation function reduces to,

$$R_{XX}(\tau) = E[X(t) \cdot X(t+\tau)] \cong E[X(t)] \cdot E[X(t+\tau)] = m_X^2 . \quad \text{(B - 6)}$$

The value of τ for which $R_{XX}(\tau)$ goes to m_X^2 represents the time separation required for the random process to become "uncorrelated", not all processes have such a τ.

For processes of interest in this work,

$$E[X(t)] = 0, \quad \forall t \quad \text{(B - 7)}$$

and there exists

$$R_{XX}(\tau) \equiv 0, \text{ for } \tau > \tau_0 . \quad \text{(B - 8)}$$

The power spectral density of a stationary random process, $X(t)$, is the *Fourier Transform* of the *autocorrelation* function,

$$S_X(\omega) = F\{R_{XX}(\tau)\} = \int_{-\infty}^{\infty} R_{XX}(\tau) \cdot e^{-j\omega\tau} d\tau . \quad \text{(B - 9)}$$

B.3 Example

The following example illustrates the above theory using a simple random binary waveform.

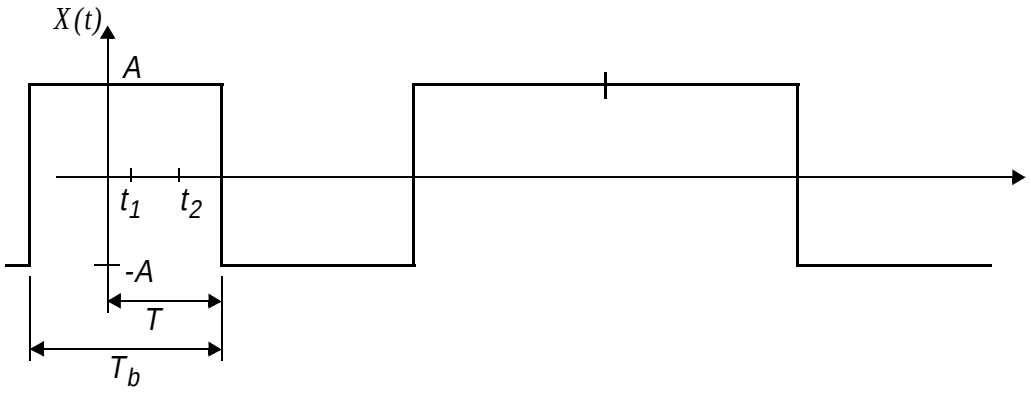

Fig. B.1: A Sample Function of the Random Binary Waveform.

The sample function $X(t)$ shown in Fig. B.1 is a random binary waveform that has the following properties: (a) each pulse is of duration T_b; (b) the two possible pulse levels $-A$ and A are equally likely, and the value of $X(t)$ in any one pulse interval is statistically independent of the values in all other intervals; (c) the starting time T of $X(t)$ is uniformly distributed over $(0, T_b)$.

In order to find the power spectral density of this random waveform, we calculate the autocorrelation function. Let t_1, t_2 be two arbitrary values of time and assume that $0 < t_1 < t_2 < T_b$, so $|t_1 - t_2| < T_b$. Then $X(t_1)$ and $X(t_2)$ are in the same pulse interval iff (see Fig. B.1)

$$t_2 \le T \le t_1 + T_b. \tag{B - 10}$$

The probability that T is within this range is

$$P(t_2 \le T \le t_1 + T_b) = \int_{t_2}^{T_b + t_1} p_T(\xi)\, d\xi = \frac{T_b + t_1 - t_2}{T_b}. \tag{B - 11}$$

Letting $\tau = t_2 - t_1$, we can rewrite this result as

$$P(t_2 \le T \le t_1 + T_b) = 1 - \frac{\tau}{T_b}. \qquad \text{(B - 12)}$$

Taking absolute values to allow negative arguments (because $R_{XX}(t_1, t_2) = R_{XX}(t_2, t_1)$), the autocorrelation function is

$$E[X(t) \cdot X(t+\tau)] = A^2 \cdot \left(1 - \frac{|\tau|}{T_b}\right), \quad |\tau| < T_b. \qquad \text{(B - 13)}$$

For $|\tau| > T_b$, the random variables $X(t_1)$ and $X(t_1 + \tau)$ are statistically independent (that is, the times, t_1 and $t_1 + \tau$, are in different pulses), and the autocorrelation is

$$E[X(t) \cdot X(t+\tau)] = m_X^2 = 0, \quad |\tau| > T_b. \qquad \text{(B - 14)}$$

Combining these results, the autocorrelation function can be written

$$R_{XX}(\tau) = A^2 \cdot \Lambda\left(\frac{\tau}{T_b}\right), \qquad \text{(B - 15)}$$

where

$$\Lambda\left(\frac{\tau}{T_b}\right) = \begin{cases} 1 + \dfrac{\tau}{T_b}, & -T_b \le \tau \le 0 \\ 1 - \dfrac{\tau}{T_b}, & 0 \le \tau \le T_b \\ 0, & otherwise \end{cases} \qquad \text{(B - 16)}$$

The power spectral density is the *Fourier Transform* of the autocorrelation function:

$$S_X(\omega) = A^2 T_b \cdot Sa^2(\omega T_b/2), \quad \text{(B - 17)}$$

where $T_b \cdot Sa^2(\omega T_b/2)$ is the Fourier Transform of $\Lambda\left(\frac{\tau}{T_b}\right)$. Re-writing Eq. B - 17 gives

$$S_X(\omega) = \frac{|\Pi(\omega)|^2}{T_b}, \quad \text{(B - 18)}$$

where $\Pi(\omega) = AT_b \cdot Sa(\omega T_b/2)$ is the *Fourier Transform* of a pulse or rectangular waveform, $rect(\tau/T_b)$.

B.4 Reference

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