# SECTION 6

# MULTICHANNEL APPLICATIONS

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- Filtering Considerations for Data Acquisition Systems
- SHA and ADC Settling Time Requirements in Multiplexed Applications
- Complete Data Acquisition Systems on a Chip
- Multiplexing into Sigma-Delta ADCs
- Simultaneous Sampling Systems
- Data Distribution Systems using Multiple DACs

# SECTION 6

# MULTICHANNEL APPLICATIONS

*Walt Kester, Wes Freeman*

## DATA ACQUISITION SYSTEM CONFIGURATIONS

There are many applications for data acquisition systems in measurement and process control. All data acquisition applications involve digitizing analog signals for analysis using ADCs. In a measurement application, the ADC is followed by a digital processor which performs the required data analysis. In a process control application, the process controller generates feedback signals which typically must be converted back into analog form using a DAC.

Although a single ADC digitizing a single channel of analog data constitutes a data acquisition system, the term *data acquisition* generally refers to multi-channel systems. If there is feedback from the digital processor, DACs may be required to convert the digital responses into analog. This process is often referred to as *data distribution*.

Figure 6.1 shows a data acquisition/distribution process control system where each channel has its own dedicated ADC and DAC. An alternative configuration is shown in Figure 6.2, where analog multiplexers and demultiplexers are used with a single ADC and DAC. In most cases, especially where there are many channels, this configuration provides an economical alternative.

**DATA ACQUISITION SYSTEM**
**USING ADC / DAC PER CHANNEL**

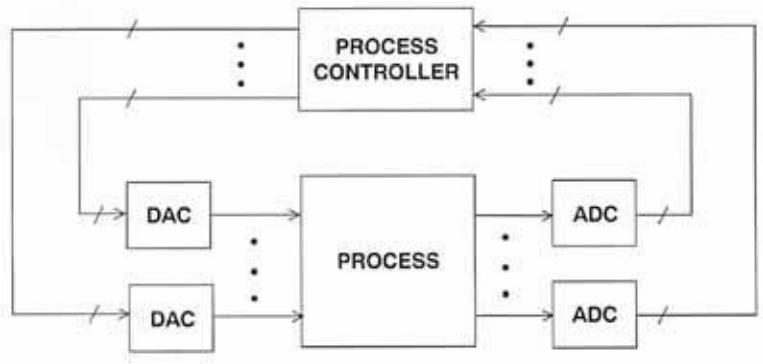



**Figure 6.1**

**DATA ACQUASITION SYSTEM USING ANALOG MULTIPLEXING / DEMULTIPLEXING AND SINGLE ADC / DAC**

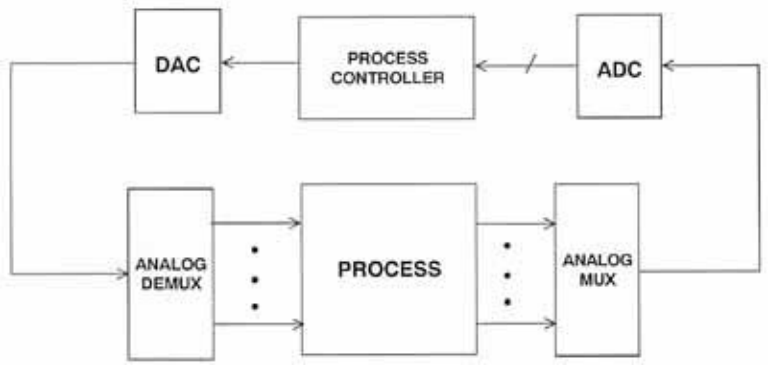



**Figure 6.2**

There are many tradeoffs involved in designing a data acquisition system. Issues such as filtering, amplification, multiplexing, demultiplexing, sampling frequency, and partitioning must be resolved.

## MULTIPLEXING

Multiplexing is a fundamental part of a data acquisition system. Multiplexers and switches are examined in more detail in Reference 1, but a fundamental understanding is required to design a data acquisition system. A simplified diagram of an analog multiplexer is shown in Figure 6.3. The number of input channels typically ranges from 4 to 16, and the devices are generally fabricated on CMOS processes. Some multiplexers have internal channel-address decoding logic and registers, while with others, these functions must be performed externally. Unused multiplexer inputs *must* be grounded or severe loss of system accuracy may result. The key specifications are *switching time*, *on-resistance*, *on-resistance modulation*, and *off-channel isolation (crosstalk).* Multiplexer switching time ranges from about 50ns to over 1µs, on-resistance from 25ohms to several hundred ohms, and off-channel isolation from 50 to 90dB. The use of trench isolation has eliminated latch-up in multiplexers while yielding improvements in speed at low supply voltages.

**SIMPLIFIED DIAGRAM OF A**
**TYPICAL ANALOG MULTIPLEXER**

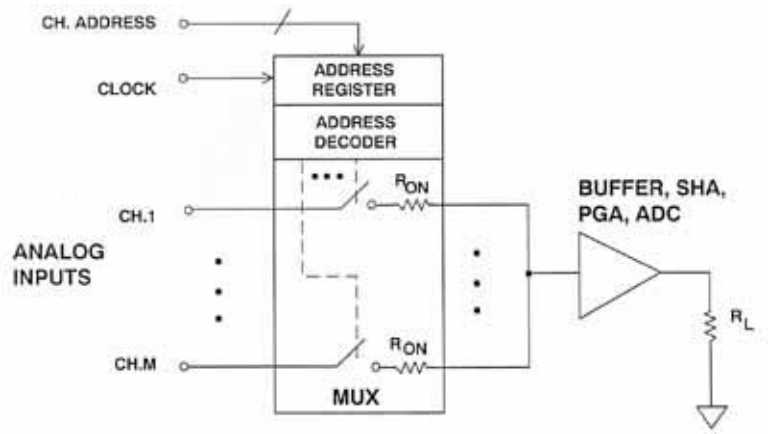



**Figure 6.3**

**MULTIPLEXER KEY SPECIFICATIONS**

- **Switching Time: 50ns to >1μs**
- **On-Resistance: 25Ω to hundreds of Ω's**
- **On-Resistance Modulation (Ron change with signal level)**
- **Off-Channel Isolation: 50 to 90 dB**
- **Overvoltage Protection**

**Figure 6.4**

**WHAT'S NEW IN MULTIPLEXERS?**

- **Trench Isolation gives high speed, latch-up protection, and low-voltage operation**

- **ADG511, ADG512, ADG513: +3.3V, +5V, ±5V specified**
  **Ron < 50Ω @ ±5V**
  **Switching Time: <200ns @ ±5V**

- **ADG411, ADG412, ADG413: ±15V, +12V specified**
  **Ron < 35Ω @**
  **±15V Switching Time: <150ns @ ±15V**

- **ADG508F, ADG509F, ADG528F: ±15V specified**
  **Ron < 300Ω**
  **Switching Time: < 250ns**
  **Fault-Protection on Inputs and Outputs**

**Figure 6.5**

Multiplexer on-resistance is generally slightly dependent on the signal level (often called $R_{on}$ modulation). This will cause signal distortion if the multiplexer must drive a load resistance, therefore the multiplexer output should therefore be isolated from the load with a suitable buffer amplifier. A separate buffer is not required if the multiplexer drives a high input impedance, such as a PGA, SHA or ADC - but beware! Some SHAs and ADCs draw high frequency pulse current at their sampling rate and cannot tolerate being driven by an unbuffered multiplexer. A detailed analysis of multiplexers can be found in Reference 1, Section 8, or Reference 2, Section 2.

An M-channel multiplexed data acquisition system is shown in Figure 6.6. The multiplexer output drives a PGA whose gain can be adjusted on a per-channel basis depending on the channel signal level. This ensures that all channels utilize the full dynamic range of the ADC. The PGA gain is changed at the same time as the multiplexer is switched to a new channel. The ADC *Convert Command* is applied after the multiplexer and the PGA have settled to the required accuracy (1LSB). The maximum sampling frequency (when switching between channels) is limited by the multiplexer switching time $t_{mux}$, the PGA settling time $t_{pga}$, and the ADC conversion time $t_{conv}$ as shown in the formula.

**MULTIPLEXED DATA AQUISITION SYSTEM WITH PGA AND SAR ADC**

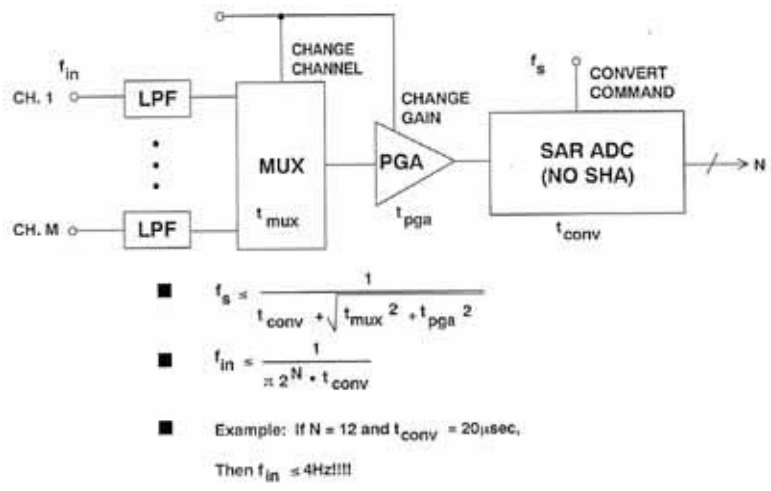



**Figure 6.6**

In a multiplexed system it is possible to have a positive fullscale signal on one channel and a negative fullscale signal on the other. When the multiplexer switches between these channels its output is a fullscale step voltage. All elements in the signal path must settle to the required accuracy (1LSB) before the conversion is made. The effect of inadequate settling is dc crosstalk between channels.

The SAR ADC chosen in this application has no internal SHA (similar to the industry-standard AD574-series), and therefore the input signal must be held constant (within 1LSB) during the conversion time in order to prevent encoding errors. This defines the maximum rate-of-change of the input signal:

$$\left.\frac{dv}{dt}\right|_{max} \leq \frac{1\,LSB}{t_{conv}}$$

The amplitude of a fullscale sinewave input signal is equal to (2^N)/2, or 2^(N-1), and its maximum rate-of change is

$$\left.\frac{dv}{dt}\right|_{max} = 2\pi f_{max} \; 2^{N-1} = \pi f_{max} \; 2^N$$

Setting the two equations equal, and solving for $f_{max}$,

$$f_{max} \leq \frac{1}{\pi \; 2^N \, t_{conv}}$$

For example, if the ADC conversion time is 20μsec (corresponding to a maximum sampling rate of slightly less than 50kSPS), and the resolution is 12-bits, then the

maximum channel input signal frequency is limited to 4Hz. This may be adequate if the signals are DC, but the lack of a SHA function severely limits the ability to process dynamic signals.

Adding a SHA function to the ADC as shown in Figure 6.7 allows processing of much faster signals with almost no increase in system complexity, since sampling ADCs such as the AD1674 have the SHA function on-chip.

**THE ADDITION OF A SHA FUNCTION TO THE ADC ALLOWS PROCESSING OF DYNAMIC INPUT SIGNALS**

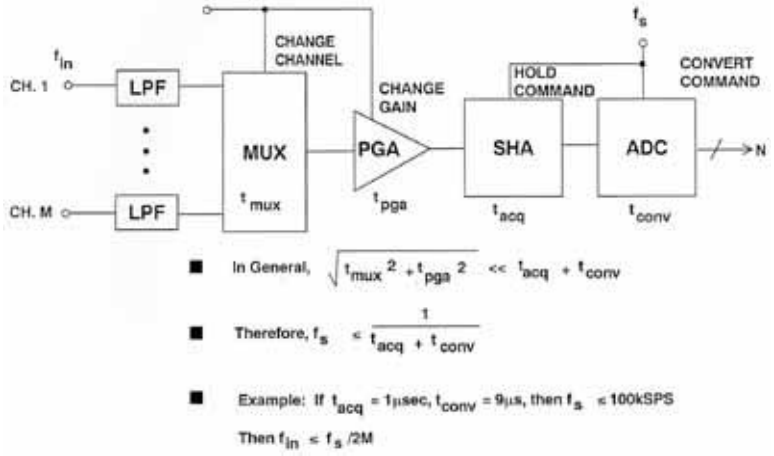



**Figure 6.7**

**TYPICAL TIMING DIAGRAM FOR MULTIPLEXED DATA ACQUISITION SYSTEM USING SHA**

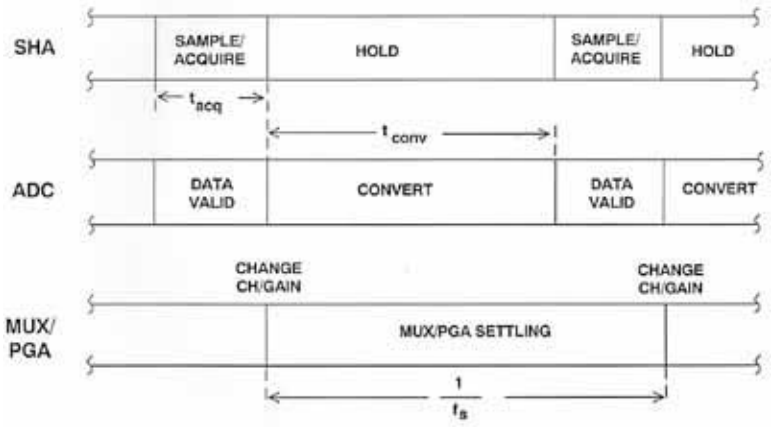



**Figure 6.8**

The timing is adjusted such that the multiplexer and the PGA are switched immediately following the acquisition time of the SHA. If the combined multiplexer and PGA settling time is less than the ADC conversion time (see Figure 6.8), then the maximum sampling frequency of the system is given by:

$$f_S \leq \frac{1}{t_{acq} + t_{conv}}$$

The AD1674 has a conversion time of 9µs, an acquisition time of 1µs to 12-bits, and a sampling rate of 100kSPS is possible, if all the channels are addressed. The per-channel sampling rate is obtained by dividing the ADC sampling rate by M.

## FILTERING CONSIDERATIONS IN DATA ACQUISITION SYSTEMS

Filtering in data acquisition systems not only prevents aliasing of unwanted signals but also reduces noise by limiting bandwidth. In a multiplexed system, there are basically two places to put filters: in each channel, and at the multiplexer output.

**FILTERING IN A DATA ACQUISITION SYSTEM**

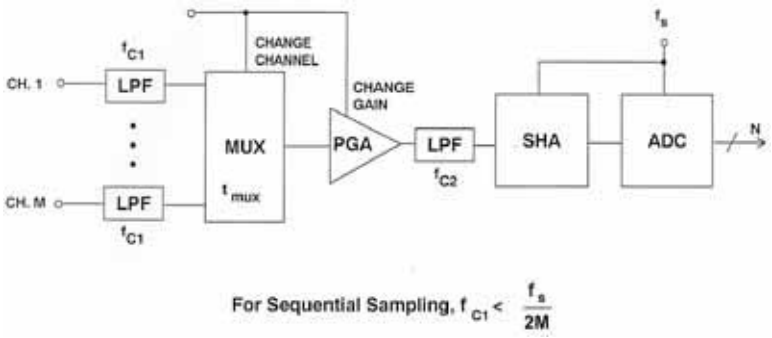



**Figure 6.9**

The filter at the input of each channel is used to prevent aliasing of signals which fall outside the Nyquist bandwidth. The per-channel sampling rate (assuming each channel is sampled at the same rate) is $f_S/M$, and the corresponding Nyquist frequency is $f_S/2M$. The filter should provide sufficient attenuation at $f_S/2M$ to prevent dynamic range limitations due to aliasing.

A second filter can be placed in the signal path between the multiplexer output and the ADC, usually between the PGA and the SHA. The cutoff frequency of this filter must be carefully chosen because of its impact on settling time. In a multiplexed system such as shown in Figure 6.7, there can be a fullscale step voltage change at the multiplexer output when it is switched between channels. This occurs if the signal on one channel is positive fullscale, and the signal on the adjacent channel is negative fullscale. From the timing diagram shown in Figure 6.8, the signal from the filter has essentially the entire conversion period ($1/f_S$) to settle from the step voltage. The signal should settle to within 1LSB of the final value in order not to introduce a significant error. The settling time requirement therefore places a lower limit on the filter's cutoff frequency. The single-pole filter settling time required to maintain a given accuracy is shown in Figure 6.10. The settling time requirement is

expressed in terms of the filter time constant and also the ratio of the filter cutoff frequency, $f_{c2}$,to the ADC sampling frequency, $f_S$.

**SINGLE-POLE FILTER SETTLING TIME TO REQUIRED ACCURACY**

| RESOLUTION, # OF BITS | LSB (%FS) | # OF TIME CONSTANTS | $f_{c2}/f_S$ |
|---|---|---|---|
| 6 | 1.563 | 4.16 | 0.67 |
| 8 | 0.391 | 5.55 | 0.89 |
| 10 | 0.0977 | 6.93 | 1.11 |
| 12 | 0.0244 | 8.32 | 1.32 |
| 14 | 0.0061 | 9.70 | 1.55 |
| 16 | 0.00153 | 11.09 | 1.77 |
| 18 | 0.00038 | 12.48 | 2.00 |
| 20 | 0.000095 | 13.86 | 2.22 |
| 22 | 0.000024 | 15.25 | 2.44 |

**Figure 6.10**

As an example, assume that the ADC is a 12-bit one sampling at 100kSPS. From the table in Figure 6.10, 8.32 time constants are required for the filter to settle to 12-bit accuracy, and

$$\frac{f_{c2}}{f_S} \geq 1.32, \text{ or } f_{c2} \geq 132\text{kSPS}.$$

While this filter will help prevent wideband noise from entering the SHA, *it does not provide the same function as the antialiasing filters at the input of each channel.*

The above analysis assumes that the multiplexer/PGA combined settling time is significantly less than the filter settling time. If this is not the case, then the filter cutoff frequency must be larger, and in most cases it should be left out entirely in favor of per-channel filters.

## SHA AND ADC SETTLING TIME REQUIREMENTS IN MULTIPLEXED APPLICATIONS

We have discussed the importance of the fullscale settling time of the multiplexer/PGA/filter combination, but what is equally important is the ability of the ADC to acquire the final value of the step voltage input signal to the required accuracy. Failure of any link in the signal chain to settle will result in dc crosstalk between adjacent channels and loss of accuracy. If the data acquisition system uses a separate SHA and ADC, then the key specification to examine is the SHA *acquisition time*, which is usually specified as a the amount of time required to acquire a fullscale input signal to 0.1% accuracy (10-bits) or 0.01% accuracy (13-

bits). In most cases, both 0.1% and 0.01% times are specified. If the SHA acquisition time is not specified for 0.01% accuracy or better, it should not be used in a 12-bit multiplexed application.

If the ADC is a sampling one (with internal SHA), the SHA acquisition time required to achieve a level of accuracy may still be specified, as in the case of the AD1674 (1µs to 12-bit accuracy). SHA acquisition time and accuracy are not directly specified for some sampling ADCs, so the *transient response* specification should be examined. The transient response of the ADC (settling time to within 1 LSB for a fullscale step input) must be less the $1/f_S$, where $f_S$ is the ADC sampling rate. This often ignored specification may become the weakest link in the signal chain. In some cases neither the SHA acquisition time to specified accuracy nor the transient response specification may appear on the data sheet for the particular ADC, in which case it is probably not acceptable for multiplexed applications. Because of the difficulty in measuring and achieving better than 12-bit settling times using discrete components, the accuracy of most multiplexed data acquisition systems is limited to 12-bits. Designing multiplexed systems with greater accuracy is extremely difficult, and using a single ADC per channel should be strongly considered at higher resolutions.

**SHA AND ADC CONSIDERATIONS IN MULTIPLEXED DATA ACQUISITION SYSTEMS**

- **Examine SHA Acquisition Time Specification to Required Accuracy:**

  **0.1% = 10-bits**
  **0.01% = 13-bits**

- **If Sampling ADC, SHA Acquisition Time may not be given, so examine Transient Response Specification**
- **Inadequate Settling Results in Loss of Accuracy and Causes DC Crosstalk Between Channels**
- **Multiplexing at greater than 12-bits Accuracy, or at Video Speeds is Extremely Difficult!**

**Figure 6.11**

## COMPLETE DATA ACQUISITION SYSTEMS ON A CHIP

VLSI mixed-signal processing allows the integration of large and complex data acquisition circuits on a single chip. Most signal conditioning circuits including multiplexers, PGAs, and SHAs, may now be manufactured on the same chip as the ADC. This high level of integration permits data acquisition systems to be specified and tested as a single complex function.

Such functionality relieves the designer of most of the burden of testing and calculating error budgets. The DC and AC characteristics of a complete data

acquisition system are specified as a complete function, which removes the necessity of calculating performance from a collection of individual worst case device specifications. A complete monolithic system should achieve a higher performance at much lower cost than would be possible with a system built up from discrete functions. Furthermore, system calibration is easier and in fact many monolithic DASs are self calibrating.

With these high levels of integration, it is both easy and inexpensive to make many of the parameters of the device programmable. Parameters which can be programmed include gain, filter cutoff frequency, and even ADC resolution and conversion time, as well as the obvious digital/MUX functions of input channel selection, output data format, and unipolar/bipolar range.

The AD7890 is an example of a highly integrated monolithic data acquisition system. It has 8 multiplexed input channels, a SHA, an internal voltage reference, and a fast 12-bit ADC. Input scaling allows up to ±10V inputs when operating on a single +5V supply. Its block diagram is shown in Figure 6.12, and key specifications are summarized in Figure 6.13. Both AC and DC parameters are fully specified, simplifying the preparation of an error budget, and three types are available with three different standard input ranges:-

| | |
|---|---|
| AD7890-10 | ±10 V |
| AD7890-5 | 0 to 5V |
| AD7890-2 | 0 to +2.5V |

**AD7890 8-CHANNEL, 12-BIT, 100kSPS COMPLETE DATA ACQUISITION SYSTEM**

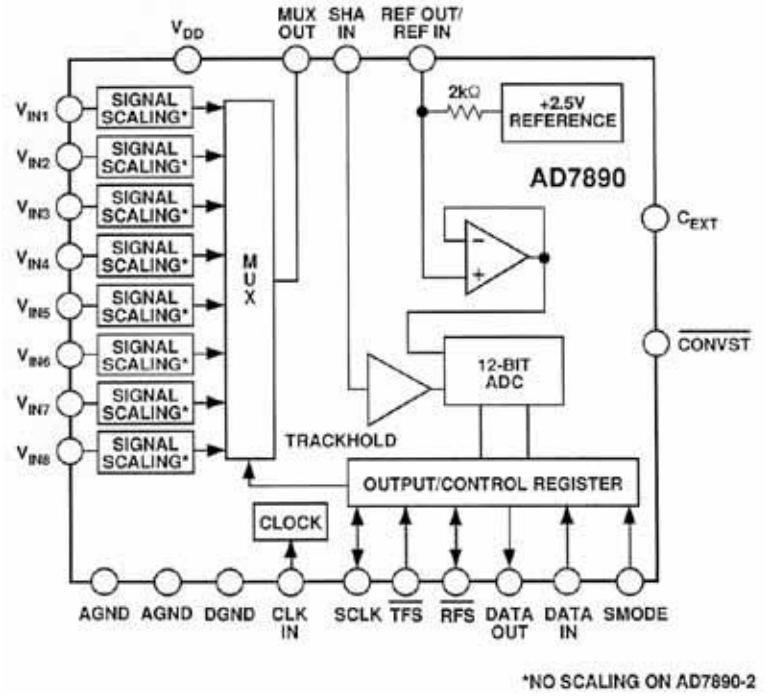



**Figure 6.12**

**AD7890 SPECIFICATIONS**

- **ADC Conversion Time:** **5.9μs**
- **SHA Acquisition Time:** **2μs**
- **117kSPS Throughput Rate** **(Includes 0.6μs Overhead)**
- **AC and DC Specifications**
- **Single +5V Operation**
- **Low Power Drain:**

| | |
|---|---|
| **Operational:** | **30mW** |
| **Power Down Mode** | **1mW** |

- **Standard Input Ranges**

| | |
|---|---|
| **AD7890 - 10:** | **±10V** |
| **AD7890 - 5:** | **0 to +5V** |
| **AD7890 - 2:** | **0 to +2.5V** |

**Figure 6.13**

The input channel selection is via a serial input port. A total of 5 bits of data control the AD7890 via a serial port:- 3 address bits select the input channel, a CONV bit starts the A-D conversion, and 1 in the STBY register places the device in a power-down mode where its power consumption is under 1mW. All timing takes place on the chip and a single external capacitor controls the acquisition time of the internal track-and-hold. A-D conversion may also be initiated externally using the CONVST pin.

With the serial clock rate at its maximum of 10MHz, the achievable throughput rate for the AD7890 is 5.9μs (conversion time) plus 0.6μs (six serial clocks of internal overhead) plus 2μs (acquisition time). This results in a minimum throughput time of 8.5μs (equivalent to a throughput rate of 117kSPS). The AD7890 draws 30mW from a +5V supply.

The entire family of AD789X 12-bit data acquisition ADCs is shown in Figure 6.14. The AD7890 and AD7891 are complete 8-channel data acquisition systems, while the AD7892, AD7893, and AD7896 are designed for use on a single channel, or with an external multiplexer.

**AD789X SERIES OF 12-BIT ADCs FOR DATA ACQUISITION**

| MODEL | AD7890 | AD7891 | AD7892 | AD7893 | AD7896 |
|---|---|---|---|---|---|
| T'Put (kSPS) | 100 | 500 | 500/600 | 117 | 100 |
| Pwr Supply | 5V | 5V | 5V | 5V | 2.7 to 5V |
| Power | 50mW | 90mW | 90mW | 45mW | 15mW @ 3.3V |
| Power Down | Yes | Yes | Yes | No | Yes |
| Interface | Serial | Parallel | Par / Ser | Serial | Serial |
| Channels | 8 | 8 | 1 | 1 | 1 |
| Pin Count | 24 | 44 | 24 | 8 | 8 |

**Figure 6.14**

The AD785X 12-bit low power data acquisition ADCs have been designed and fully specified for either +3V or +5V operation. This family includes parallel and serial single and 8-channel versions. The devices have self or system calibration modes for offset, gain, and the internal SAR DAC.

**AD785X SERIES OF 3V / 5V 12-BIT ADCs**

| MODEL | AD7853 (AD7853L) | AD7854 (AD7854L) | AD7858 (AD7858L) | AD7859 (AD7859L) |
|---|---|---|---|---|
| T'Put (kSPS) | 200 (100) | 200 (100) | 200 (100) | 200 (100) |
| Pwr Supply | +3V, +5V | +3V, +5V | +3V, +5V | +3V, +5V |
| Power, +3V | 15mW (5.5mW) | 15mW (5.5mW) | 15mW (5.5mW) | 15mW (5.5mW) |
| Power Down | Yes | Yes | Yes | Yes |
| Interface | Serial | Parallel | Serial | Parallel |
| Channels | 1 | 1 | 8 | 8 |
| Pin Count | 24 | 28 | 24 | 40 / 44 |

( ) VALUES FOR LOW POWER, L, VERSIONS

**Figure 6.15**

## MULTIPLEXING INPUTS TO SIGMA-DELTA ADCS

As was discussed in Section 3, the digital filter is an integral part of a sigma-delta ADC. When the input to a sigma-delta ADC changes by a large step, the entire digital filter must fill with the new data before the output becomes valid, which is a slow process. This is why sigma-delta ADCs are sometimes said to be unsuitable for multi-channel multiplexed systems - they are not inherently so, but the time taken to change channels can be inconvenient.

As an example, the AD7710-family of ADCs contains an on-chip multiplexer (see Figure 6.16), and the digital filter (frequency response shown in Figure 6.17)

requires three conversion cycles (300ms at a 10Hz throughput rate) to settle. It is thus possible to multiplex sigma-delta converters, provided adequate time is allowed for the internal digital filter to settle.

**THE AD771X-SERIES PROVIDES A HIGH LEVEL OF INTEGRATION IN A 24-PIN PACKAGE**

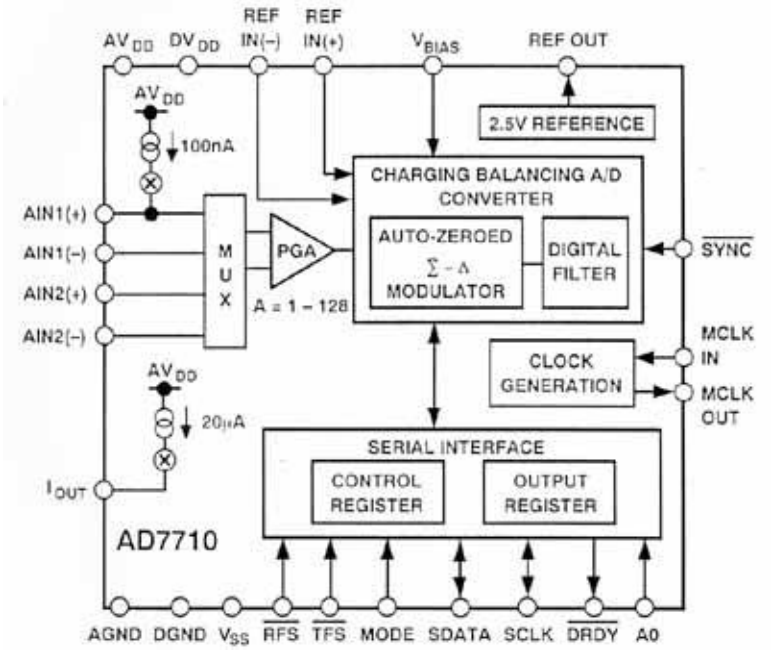



**Figure 6.16**

**AD7710 DIGITAL FILTER FREQUENCY RESPONSE**

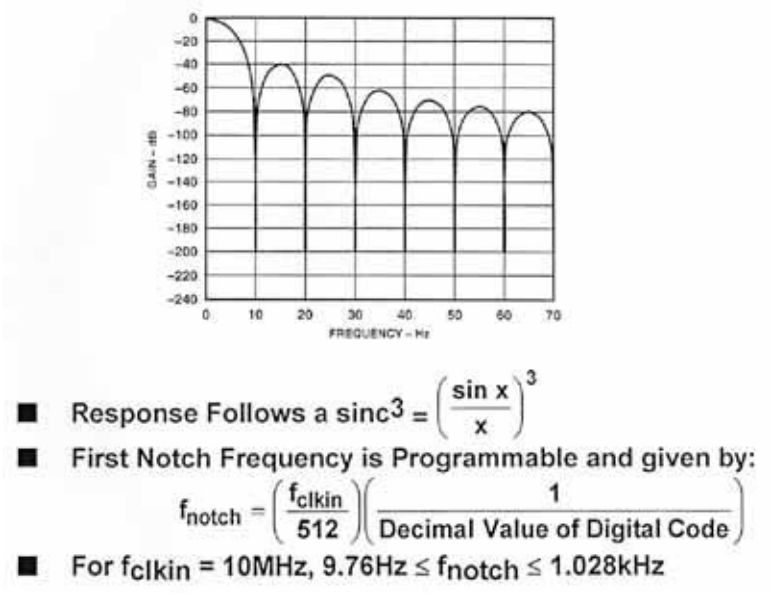



**Figure 6.17**

**THE RATE OF CONVERSION AND SETTLING TIME DEPENDS ON THE FILTER SETTING**

| | FILTER NOTCH FREQUENCY (Hz) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | 10 | 25 | 30 | 50 | 60 | 100 | 250 | 500 | 1k |
| CONVERSION TIME (ms) | 100 | 40 | 33.3 | 20 | 16.7 | 10 | 4 | 2 | 1 |
| MUX SWITCHING OR FULLSCALE WITH $\overline{\text{SYNC}}$, SETTLING TIME (ms) | 300 | 120 | 100 | 60 | 50 | 30 | 12 | 6 | 3 |
| ASYNCHRONOUS FULLSCALE SETTLING TIME (ms) | 400 | 160 | 133.3 | 80 | 66.7 | 40 | 16 | 8 | 4 |

- Conversion Time = $\frac{1}{\text{Filter Notch Frequency}}$
- Digital Filter Requires Settling Time for Input Step Changes
- Use $\overline{\text{SYNC}}$ Input to Decrease Settling Time

**Figure 6.18**

In the case of the AD771X-series, four conversions must take place after a channel change before the output data is again valid (Figure 6.18). The SYNC input pin resets the digital filter and, if it is used, data is valid on the third output afterwards, saving one conversion cycle. When the internal multiplexer is switched, the SYNC is automatically operated.

If sigma-delta ADCs are used in multi-channel applications, consider using one sigma-delta ADC per channel as shown in Figure 6.19. This eliminates the requirement for an analog multiplexer but requires that the outputs be synchronized in simultaneous sampling applications. Although the inputs are sampled at the same instant at a rate $Kf_S$, the decimated output frequency, $f_S$, is generally derived internally in each ADC by dividing the input sampling frequency by K (the oversampling rate). The output data must therefore be synchronized by the same clock at a frequency $f_S$.

## SYNCHRONIZING MULTIPLE SIGMA-DELTA ADCs IN SIMULTANEOUS SAMPLING APPLICATIONS

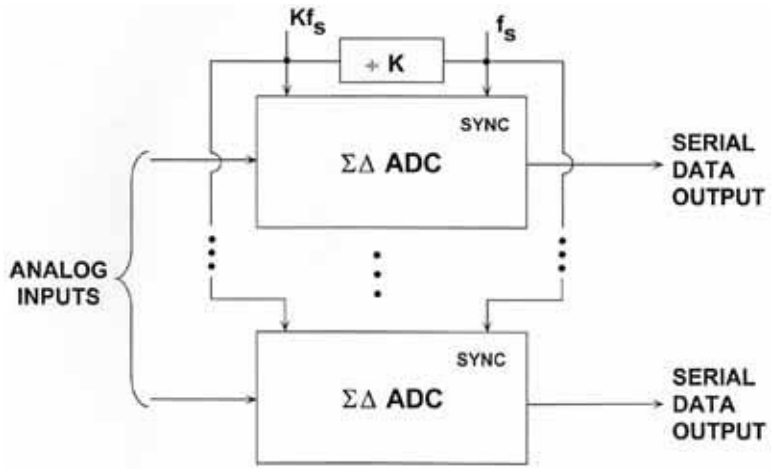



**Figure 6.19**

Products such as the AD7716 include multiple sigma-delta ADCs in a single IC, and provide the synchronization automatically. The AD7716 is a quad sigma-delta ADC with up to 22-bit resolution and an over-sampling rate of 570kSPS. A functional diagram of the AD7716 is shown in Figure 6.20 and some of its key features in Figure 6.21. The device does not have a "start conversion" control input, but samples continuously. The cutoff frequency of the digital filters (which may be changed during operation, but only at the cost of a loss of valid data for a short time while the filters clear) is programmed by data written to the DAS. The output register is updated at a rate which depends on the cutoff frequency chosen. The AD7716 contains an auto-zeroing system to minimize input offset drift.

**AD7716 22-BIT QUAD SIGMA-DELTA ADC**

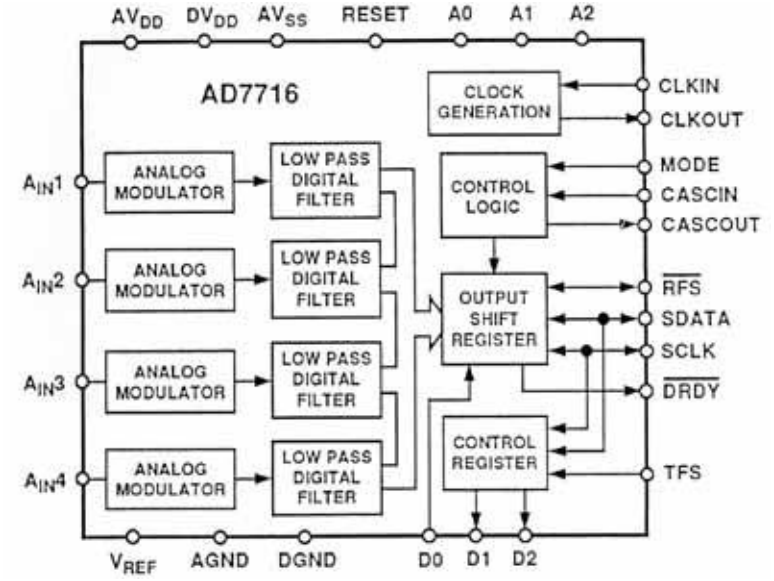



**Figure 6.20**

**AD7716 QUAD SIGMA-DELTA ADC KEY FEATURES**

- **Up to 22-Bit Resolution, 4 Input Channels**
- **ΣΔ Architecture, 570kSPS Oversampling Rate**
- **On-Chip Lowpass Filter, Programmable from 36.5Hz to 584Hz**
- **Serial Input / Output Interface**
- **±5V Power Supply Operation**
- **Low Power: 50mW**

**Figure 6.21**

## SIMULTANEOUS SAMPLING SYSTEMS

There are certain applications where it is desirable to sample a number of channels simultaneously such as in-phase and quadrature (I and Q) signal processing. A typical configuration is shown in Figure 6.22. Each channel requires its own filter and SHA. Each SHA is simultaneously placed in the *hold* mode by a common command signal. During the input SHAs' hold time the multiplexer is sequentially switched from channel to channel, and the single non-sampling ADC is used to digitize the signal on each channel. The maximum ADC sampling rate is the reciprocal of the sum of the multiplexer settling time, $t_{mux}$, and the ADC conversion time, $t_{conv}$.

$$f_{S2} \leq \frac{1}{t_{mux} + t_{conv}}$$

The maximum per-channel sampling frequency is determined by M, $t_{mux}$, $t_{conv}$, and the acquisition time of the simultaneous SHAs, $t_{acq1}$.

$$f_{S1} \leq \frac{1}{t_{acq1} + M\left(t_{mux} + t_{conv}\right)}$$

**SIMULTANEOUSLY SAMPLED DATA ACQUISITION SYSTEM USING NON-SAMPLING ADC**

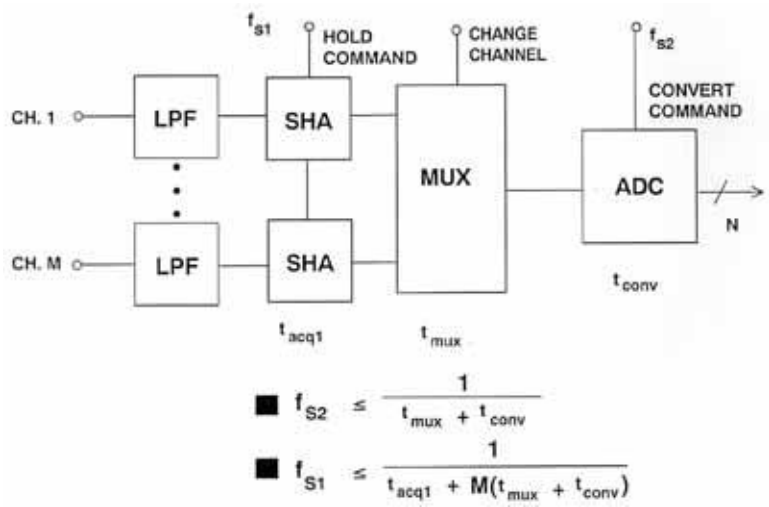



**Figure 6.22**

If a sampling ADC is used to perform the conversion (see Figure 6.23), the acquisition time of the second SHA, $t_{acq2}$, must be considered in determining the maximum ADC sampling rate, $f_{S2}$. The multiplexer should be switched to the next channel after the single SHA goes into the hold mode. If the multiplexer settling time is less than the ADC conversion time, then the maximum ADC sampling rate $f_{S2}$ is the reciprocal of the sum of the SHA acquisition time and the ADC conversion time.

$$f_{S2} \leq \frac{1}{t_{acq2} + t_{conv}}$$

The maximum input sampling frequency is less than this value divided by M, where M is the number of channels. Additional timing overhead ($t_{acq1}$) is required for the simultaneous SHAs to acquire the signals.

$$f_{S1} < \frac{1}{t_{acq1} + M\left(t_{conv} + t_{acq2}\right)}$$

**SIMULTANEOUS SAMPLING DATA ACQUISITION SYSTEM USING SAMPLING ADC**

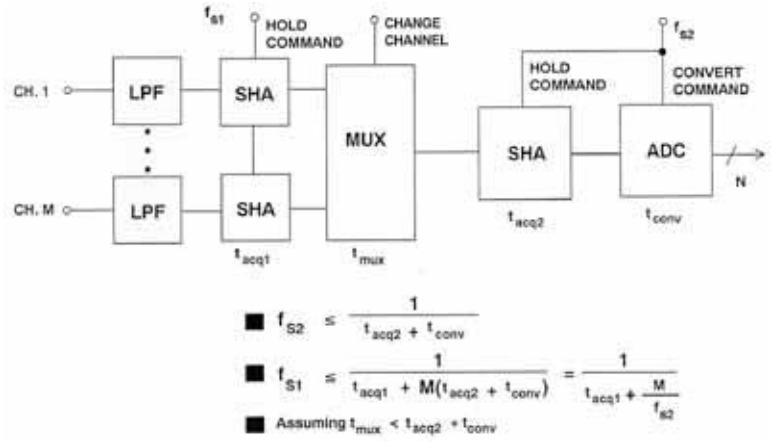



**Figure 6.23**

## USING MULTIPLE-DACS TO SIMPLIFY DATA DISTRIBUTION SYSTEMS

***Wes Freeman***

In many industrial and process control applications, multiple programmable voltage sources are required. Traditionally, these applications have required a large number of components, but recent product developments have greatly reduced the parts count without compromising performance.

**DATA DISTRIBUTION SYSTEM USING MULTIPLE DACs**

- **Many systems require multiple, programmable voltages**
  - **Automatic Test Equipment (ATE)**
  - **Robotics**
  - **Industrial Automation**
  - **System Calibration**
  - **Ultrasound/Sonar Power Gain and Receiver Level**

**Figure 6.24**

Multiple voltage outputs can either be derived by demultiplexing the output of a single DAC or by employing multiple DACs. These two approaches are shown in Figure 6.25. In the demultiplexed circuit, one DAC feeds the inputs of several sample-and-hold amplifiers (SHA). The equivalent digital value for the analog output is applied to the DAC, and the appropriate SHA is selected. After the DAC settling time and SHA acquisition time requirements have been met, the SHA can be deselected and the next channel updated. Once a SHA is deselected, the output voltage will begin to droop at a rate specified for the SHA. Thus, the SHA must be refreshed before the output voltage droop exceeds the required accuracy (typically 1/2 LSB).

## OPTIONS FOR ANALOG DATA DISTRIBUTION

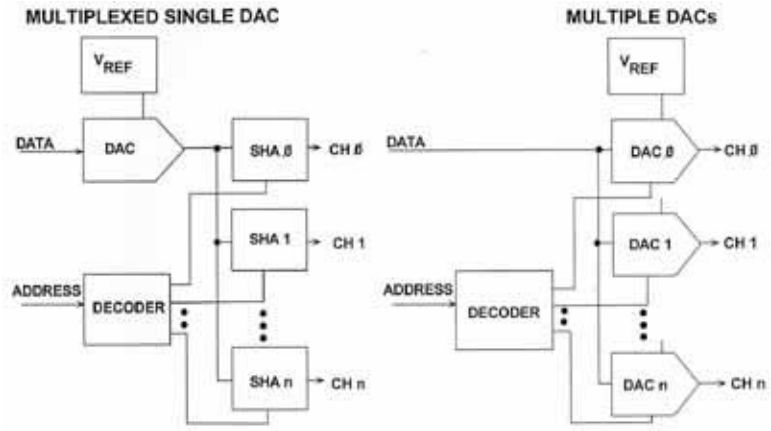



**Figure 6.25**

The multiple DAC application is straightforward. One DAC is provided for each channel, and an address decoder simply selects the appropriate DAC. No refresh is required.

The DAC plus SHA system evolved because, in the past, DACs were more expensive than SHAs. This situation was particularly true for DACs with resolution above 8 bits. In addition, multiple-SHAs with on-chip hold capacitors reduced the parts count, printed circuit board area, and cost of demultiplexed DAC systems. Finally, the demultiplexed DAC only requires one calibration step, since the same DAC provides the output voltage for each of the output channels. Of course, single-calibration is only valid if the SHA does not introduce unacceptable errors. For example, the SMP08 is an 8-channel SHA which exhibits a 10mV maximum offset voltage and is accurate to 1/2 LSB when demultiplexing an 8-bit, 5V full-scale DAC.

### WHY DEMULTIPLEX A SINGLE DAC?

- **Cost of DAC > Cost of SHA**
- **Multichannel SHAs (e.g. SMP-08/SMP-18) Reduce Parts Count**
- **Only One Calibration Required**

**Figure 6.26**

A representative 16-channel, 8-bit demultiplexed data distribution system is shown in Figure 6.27. The DAC8228 produces a voltage output which is applied to the input of 16 SHAs. The DAC digital value is written into the DAC8228 at the same time as the channel address is presented to the SHA. After the SHA's acquisition time requirement has been satisfied, the next channel can be refreshed. The SMP08's acquisition time to 0.1% is 7µs, so the maximum data transfer rate is the reciprocal of the acquisition time, or 140kHz.

## A 16-CHANNEL 8-BIT DATA DISTRIBUTION SYSTEM USING A SINGLE MULTIPLEXED DAC

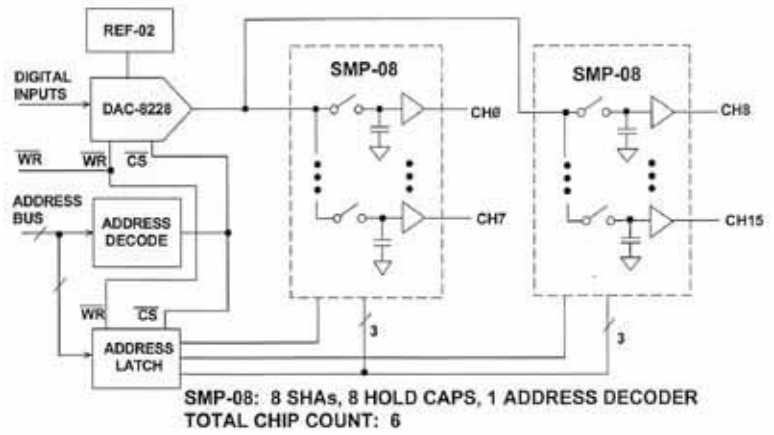



**Figure 6.27**

Once a SHA channel is deselected, the input bias current of the amplifier begins to discharge the hold capacitor. The rate at which the capacitor voltage changes is specified on the SHA data sheet as the *droop rate*. With a maximum droop rate of 20mV/s, the SMP08 can maintain 8-bit accuracy (1/2 LSB at 5V full scale) provided refreshing occurs once each 500ms.

The SMP08 is a complete, single-chip 8-channel SHA, which incorporates analog switches, hold capacitors, amplifiers, and address decoders. Each SMP08 replaces 17 components (8 SHAs, 8 hold capacitors, and one decoder). Even with this level of integration, however, the complete data distribution circuit still requires six components.

Operation of the demultiplexed DAC is shown in Figure 6.28. With the DAC output at 5V, the system refreshes CH0 once each second. The upper trace is the address decode output which goes low to select CH0. The lower trace is the output of CH0's SHA. While the address input is low, the DAC's output is connected to the input of CH0's SHA. When the address input goes high, the SMP08 maintains less than 1/4 LSB error for one second. Thus, the droop rate of this particular SMP08 is about 2mV/sec. The photo also shows a 1mV hold step when switching from sample to hold mode.

## REFRESHING THE MULTIPLEXED DAC

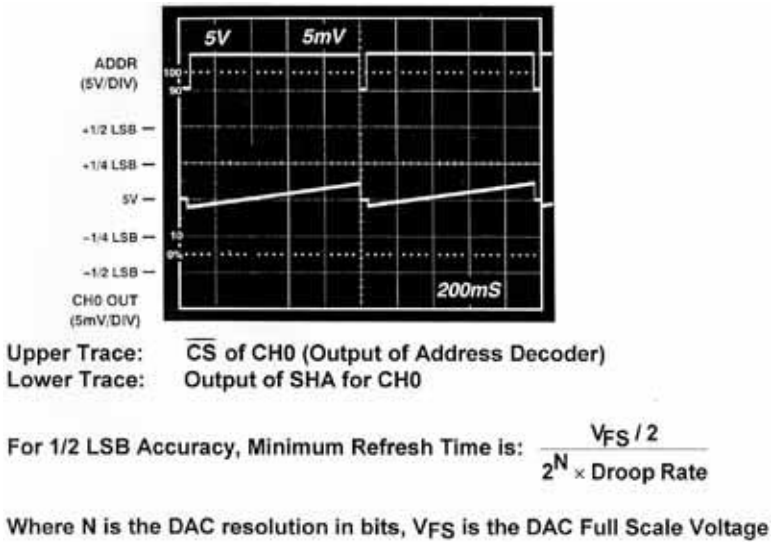



**Figure 6.28**

At first glance, demultiplexed DAC systems may appear to be more cost-effective than multiple DACs. However, several factors combine to reduce the system cost when a multiple DAC is used (Figure 6.29). For example, advances in integrated circuit fabrication, trimming and testing have combined to improve yields and reduce costs. Process improvements produce transistors and resistors with better matching, which reduces trimming requirements. At the same time, improvements in laser trimming and testing permit more accurate matching of multiple devices on one die. While these advances also have an effect on the costs of demultiplexed systems, the economics of IC fabrication are such that the impact of improvements is relatively greater on multiple DAC devices. As a result of these improvements, multiple DACs are very cost competitive with demultiplexed systems on a per-channel basis.

**WHY USE A MULTIPLE-DAC SOLUTION?**

- **Cost**
  - **Laser Trimming Aids Matching**
  - **Lower Parts Count**
  - **Reduced Design Time**
- **Additional System Features**
  - **Less Microcontroller Overhead**
  - **Faster Update Rate**
  - **Synchronized Outputs**
  - **Power-On Reset**
  - **Read-Back Capability**
  - **Serial Interface**

**Figure 6.29**

Another advantage of the multiple-DAC system is reduced parts count. While cost estimates may vary, the advantages of eliminating components in a design cannot be ignored. Among these advantages are reduced pin count, printed circuit board area, inventory, incoming inspection, and purchasing transactions.

Reducing design time also contributes to cost savings. From a design engineering point of view, design time is both a critical and a very visible factor in the "time-to-market" equation. Reducing parts count can have a major impact on design time by reducing device evaluation time, interface timing analyses, error budget analyses, printed circuit board layout, etc.

The real advantages of the single-chip multiple DAC, however, lie in the features that are difficult or impossible to add with a demultiplexed circuit. These advantages include:

1. *No refresh cycle is required*. As previously mentioned, the demultiplexed DAC must constantly be refreshed. The minimum time between refresh cycles is set by the required system accuracy (typically 1/2 LSB), SHA droop rate, and LSB voltage value. Specifically,

$$\text{Minimum Refresh Time} = \frac{V_{FS}/2}{2^N \times \text{Droop Rate}}$$

where $V_{FS}$= DAC full scale voltage and
N = DAC resolution in bits.

Constantly refreshing a demultiplexed DAC puts a software burden on the system. In particular, notice that the refresh time is halved for each additional bit of resolution. For example, if the DAC resolution is increased from 8-bits to 12-bits the

DAC must be refreshed 16 times more often. Software burden vs. hardware savings tradeoffs must be evaluated carefully in high resolution systems.

2. *Faster data update rates are possible.* In addition to requiring constant refresh, the rate at which the multiplexed DAC can be updated is limited by the sequential architecture of the system. Thus, the acquisition time of the SHA is multiplied by the number of channels. For the circuit of Figure 6.27, the best-case time for updating all 16 DAC values, assuming a 7μs SHA acquisition time, will be:

$$t_S = 16 \cdot 7\mu s = 112\mu s$$

Multiple DACs, on the other hand, can usually be treated as memory or input/output locations, and updated at or near the maximum cycle time of the microcontroller. Consecutive DACs can be loaded with data while previously-loaded DACs are settling to their final values. Since the digital transfer rate is usually faster than the settling time of the DAC, the multiple-DAC system update rate is much faster than the demultiplexed DAC rate.

3. *Multiple DACs can offer synchronized outputs.* Servo, ATE, and other systems can benefit from multiple outputs which change simultaneously. Many multiple DACs, such as the quad 8-bit AD7225 and octal 12-bit AD7568, are double-buffered. Data can be loaded into storage latches sequentially, then transferred simultaneously to the DAC latches when a separate "load" pin is brought low. For higher throughput, new data can be loaded into the storage latches as soon as the "load" pin returns high. In this case, the new data is loaded during the settling time of the DACs, so the throughput rate is maximized.

4. *Multiple DACs usually have a power-on reset feature.* Many systems must assume a known state upon power-up. For example, a programmable power supply should not output random voltages when turned on. Several DACs, such as the quad 12-bit DAC8412/DAC8413 and octal 8-bit DAC8800, provide a reset feature which sets all of the DACs to a known state. In most cases, the DAC output is reset to zero. The DAC8412, however, will reset to mid-scale. This feature provides a zero-volt output at reset when the DAC is configured for a bipolar output.

5. *Some multiple DACs' registers feature data readback.* On some multiple DACs, the data bus is actually bi-directional, and the value written into the DAC register can also be read back by the controller. This feature provides the opportunity for hardware and software error checking. Since the DAC values do not have to be saved by the controller, additional data storage is also available for minimum-memory microcomputer applications.

6. *To save real estate and parts count, some multiple DACs use serial data interfaces.* Only two or three pins are required, at both the controller and the DAC, to transfer data. Creating a serial data interface for a demultiplexed-DAC system requires several additional packages to decode the serial address, even if a serial-input DAC is specified. Dramatic reductions in pin count can be obtained when a multiple DAC with serial input is specified. For example, the DAC8420 provides four, 12-bit voltage output DACs in one 16-pin package.

A serial data interface is inherently slower than a parallel interface. While this is usually a problem only in high speed systems, the slower serial data rate does exacerbate the demultiplexed-DAC's refresh requirements.

A two chip solution to the data distribution challenge is shown in Figure 6.30. The AD8600 is a multiple-channel DAC which combines 32 registers, 16 DACs, 16 voltage output buffers, control logic, and an address decoder in a single 44-pin package.

**A 16-CHANNEL 8-BIT DATA DISTRIBUTION SYSTEM USING A 16-CHANNEL DAC**

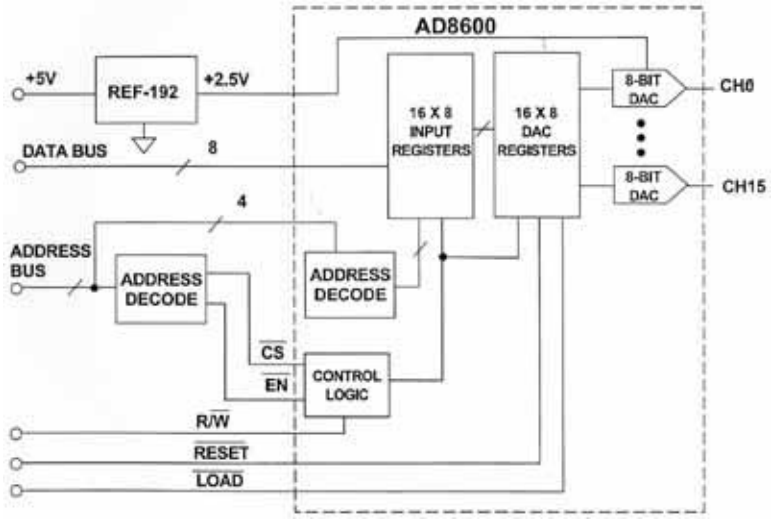



**Figure 6.30**

Interfacing to the AD8600 is easy. The DACs are simply treated as 16 memory or I/O locations. Updating the value of any DAC is merely a matter of writing the DAC value, via an 8-bit data bus, to the appropriate address. If desired, data can be written into the input registers without affecting the DAC values. When the LOAD input is pulled low, all DAC outputs will change simultaneously. Holding LOAD low causes the output of each DAC to change as soon as the WRITE command occurs.

This 16-channel, single chip DAC reduces parts count by 66% over the demultiplexed DAC solution. Inventory and assembly costs, printed circuit board area, and design time are all reduced. Refreshing the DAC values is not required, so software overhead is eliminated.

When evaluated solely on the cost of components, the demultiplexed single DAC approach is about 40% less expensive than the multiple DAC. On a system cost basis, however, the advantages of the multiple DAC make it the cost as well as the performance winner. A comparison of the two approaches is shown in Figure 6.31. The cost advantages of the DAC8300 solution include:

**COMPARING REPRESENTATIVE 16-CHANNEL, 8-BIT DATA DISTRIBUTION SYSTEMS**

| FEATURE | SINGLE DEMULTIPLEXED DAC | MULTIPLE DAC |
|---|---|---|
| Design Time | Moderate | Low |
| Refresh Required | Yes | No |
| Refresh Ripple at Output | Dependent on Refresh Rate | None |
| Synchronized Outputs | No | Yes |
| Time Required to Change All 16 DACs | 112 µs | 3.3 µs |
| Power-On Reset | No | Yes |
| Read-Back Capability | No | Yes (Available on some) |
| Serial Data Interface | Additional Components | Yes, on Some DACs |
| Parts Count | 6 | 2 |
| PC Board Holes (Total Number of Pins) | 74 | 52 |

**Figure 6.31**

1. *Reduced design time.* All of the DAC system specifications are defined in the multiple DAC data sheet. The demultiplexed DAC, on the other hand, requires analysis of the DC and AC parameters of both the DAC and SHA, as well as the relationship between these parameters. (For example, must the DAC settling time be added to the SHA acquisition time, or, since the DAC settling time is only 2µs compared to 7µs for the SHA, can the DAC settling time be ignored? Updating each channel in 7µs instead of 9µs reduces refresh overhead by about 20%, but this is only valid if system specifications are met. Clearly, prototype evaluation is required).

2. *Parts count is reduced by 66%.* As previously mentioned, costs for purchasing, inventory and assembly are reduced.

3. *The number of PC board holes (that is, the pin count) is reduced.* The number of holes that are required in the PC board is another measure of assembly cost. On this basis, the multiple DAC wins by about 30%

4. *No refresh is required*. This fact eliminates the software required to provide timing for the demultiplexed DAC, and may also free up the use of a timer on the microcontroller.

Although the cost savings listed above are significant, the multiple DAC's improvements to system performance are even more important in most applications. The system improvements include:

1. *Reduced output ripple.* The demultiplexed DAC output will always have ripple, caused by the droop rate of the SHA.

2. *Faster update rate.* The delay time imposed by the SHA acquisition time is eliminated, so the AD8600 circuit can load new DAC values in as little as 80ns. To update 16 DACs, including an 80ns load pulse to change all DAC outputs simultaneously, and allowing 2µs for DAC settling, requires:

$$t_S = (16 + 1) \cdot 80ns + 2\mu s = 3.3\mu s.$$

The demultiplexed DAC, as was shown previously, is limited by the fact that the acquisition time of the SHA is multiplied by the sequential architecture of the system. The multiple DAC has reduced the refresh time from 112µs to only 3.3µs. In applications such as automatic test equipment, the effects of a 3300% improvement in test value update time are significant. The demultiplexed DAC circuit can be improved somewhat by specifying faster SHAs, but the increased droop rate of a faster SHA will demand that refresh be performed even more frequently. The increased refresh may offset the speed advantage of the faster SHA.

3. *Simultaneous DAC output changes*. With double-buffered data latches, each of the DAC values can be loaded sequentially, but the outputs will change simultaneously. If desired, of course, any of the DACs can be updated individually.

4. *A DAC reset input*. At system power up, or during power fault recovery, setting the reset input to a logic low will force all DAC registers into the zero state. This will asynchronously place zero-volts on all of the DAC outputs.

5. *Data readback*. The DAC has a bi-directional data bus, so that the value written into the DAC register can also be read back by the controller. This feature provides the opportunity for hardware and software error checking and can be especially useful during system debugging. Since the DAC values do not have to be saved in memory by the controller, an additional 16 bytes of data storage is also available for minimum-memory microcomputer applications.

Multiple DACs are offered in a wide variety of configurations, resolution, digital interface, and analog output. For example, dual, quad, and octal versions of both 8-bit and 12-bit devices are available. Serial data interfaces are also available, for reduced pin count. A 1994 selection guide (Reference 5) from Analog Devices contains 12 multiple DAC products which have a serial data interface.

Many multiple DACs are used in automatic calibration or system nulling applications. A typical device for these tasks is the AD8842, an octal 8-bit TrimDAC® (Figure 6.32). This device includes a serial data input for DAC data and address, eight DAC registers, and eight voltage-output DACs.

## AD8842 OCTAL 8-BIT SERIAL INPUT TrimDAC®

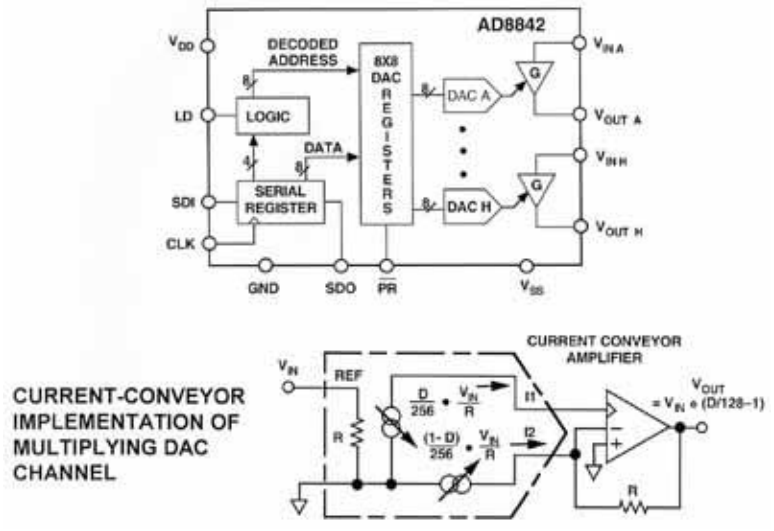



**Figure 6.32**

This device introduces a capability which is impossible with a demultiplexed DAC: *the ability to have different reference voltages for each DAC channel.* The output voltage of each channel of the AD8842 is simply:

$$V_{OUT} = V_{IN} \cdot \left(\frac{D}{128} - 1\right)$$

where D is a representation of the DAC input value (that is, 0 to 255 for an 8-bit DAC). The value of $V_{IN}$ can be either positive or negative, DC or AC, allowing each DAC a 4-quadrant multiplying capability. Since $V_{IN}$ can be an AC signal, the DACs can be also be used as a programmable gain control for signals up to 50kHz. $V_{IN}$, the analog input, exhibits a fixed input resistance of about 20kohms, so driving it, either from a DC voltage reference or from an AC source, is easy.

The AD8842 is an example of the reduction in pin count which is possible when a serial data interface is used. It combines 8 voltage output DACs, under 3-wire serial interface and an asynchronous preset input, into a single 24-pin DIP or SOIC package. To update any DAC, the DAC output value and address are shifted into the serial input register. A logic LOW on the LD input then transfers the data to the appropriate DAC register. The last bit of the serial input shift register is also available on the serial data output, so that multiple AD8842s can be daisy-chained without additional logic. Although the digital data can be loaded at an 8MHz rate, each DAC output requires 5.4µs to settle to ± 1 LSB.

Other key features of the AD8842 are shown in Figure 6.33. The preset (PR) input can be used to force the outputs of all the DACs to 0V when power is first applied, or after a power fault. Placing a logic low on PR will force a value of 128 base10 (80

base16) into all of the DAC registers. As can be seen from the output voltage equation shown in Figure 6.32, a DAC value of 128 base 10 produces a 0V output.

**AD8842 KEY FEATURES**

- **Eight Individual Channels**
- **3-Wire Serial Data Input, 8MHz Loading Rate**
- **Asynchronous Reset Input**
- **50kHz, 4-Quadrant Multiplexing Bandwidth**
- **Replaces 8 Potentiometers**
- **Constant 20kΩ Input Resistance**
- **±4V Output Swing**
- **Low Power: 95mW on ±5V Supplies**
- **24-pin Narrow DIP or SO Package**

**Figure 6.33**

The AD8842 TrimDAC® can also replace 8 potentiometers in voltage nulling applications. Unlike a trimming potentiometer, however, the TrimDAC® can generate both positive and negative voltages from a positive reference voltage. This is a significant advantage in many applications, because the nulling voltage can be derived from a very stable system reference voltage. Obtaining a bipolar nulling voltage with a potentiometer normally requires either providing two separate positive and negative reference voltages, or connecting one end of the pot to the negative power supply. Since power supplies are typically noisy and poorly regulated when compared to the system reference voltage, performance will be degraded if the power supply must be used.

The effect of a serial interface on pin count becomes even more evident as the DAC resolution increases. For example, the AD8522 squeezes two 12-bit DACs, a 2.5V reference, a double-buffered serial input, and two reset control inputs into a single 14-pin package (Figure 6.34). A companion part, the AD8582, has similar features but requires 24 pins because it has a parallel interface.

**AD8522: WORLD'S SMALLEST (SO-14, PDIP-14)**
**COMPLETE DUAL 12-BIT DAC**

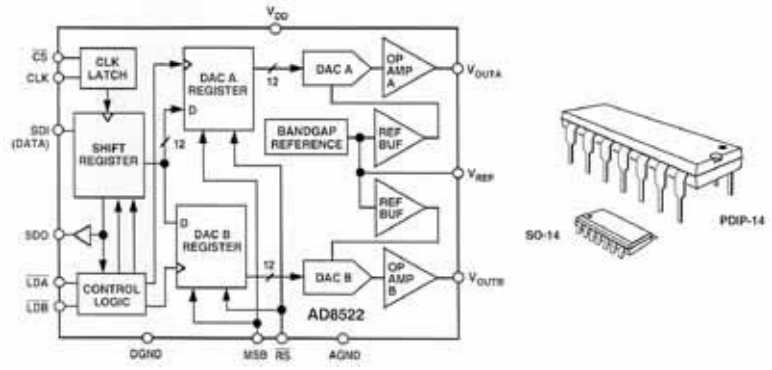



**Figure 6.34**

The AD8522's 2.5V reference is available on the $V_{REF}$ pin to provide a reference for other data acquisition portions of the system or for ratiometric applications. The reference output can also be used to create a virtual ground for applications where a quasi-bipolar output is desired. The $V_{REF}$ pin cannot, however, be used as a reference input.

As with the AD8842 octal DAC, both AD8522 DAC registers can be asynchronously forced to a half-scale value (2048 base 10 or 800 base 16). This action sets a 0V reading for quasi-bipolar applications. Both registers of the AD8522 can also be reset to a "000" value, which provides a 0V reset for unipolar applications. Other key features of the AD8522 are shown in Figure 6.35.

**AD8522 KEY FEATURES**

- **Space-Saving SOIC-14 Package, only 1.5mm Height!**
- **Low Power: 10mW max**
- **No External Components, No Adjustments Necessary**
- **+5V Operation Guaranteed Down to 4.5V Minimum**
- **4.095V Full Scale (1mV/LSB), Fully Trimmed**
- **Buffered Rail-to-Rail Voltage Outputs**
- **2.5 V VREF Output Pin - Useful for establishing virtual ground in bipolar applications**
- **Midscale or Zero-Scale Present**
- **Double-Buffered 3-Wire Serial Data Input**
- **Software and Hardware A/B DAC Select**

**Figure 6.35**

The AD8522 introduces two new concepts to the multi-channel data distribution discussion. The first new concept is the *complete* DAC (Figure 6.36). All of the systems mentioned previously have required a separate external reference, which had to be adjusted to set the DAC's full scale output voltage. The AD8522, on the other hand, has an on-chip bandgap reference which is laser-trimmed during production to provide a full scale output voltage of 4.095V (that is, 1mV/LSB). Since the voltage reference, DAC, and voltage output amplifiers are on a single chip, the entire DAC system specification is contained in the AD8522's data sheet specifications. This eliminates the necessity of evaluating several separate devices, as well as calculating the error contributions of each device, and further demonstrates the significant reduction in design time which results from reducing package count. In addition, system cost is reduced and reliability is improved because the calibration operation is eliminated.

**EQUIVALENT SCHEMATIC OF AD8522 ANALOG SECTION**

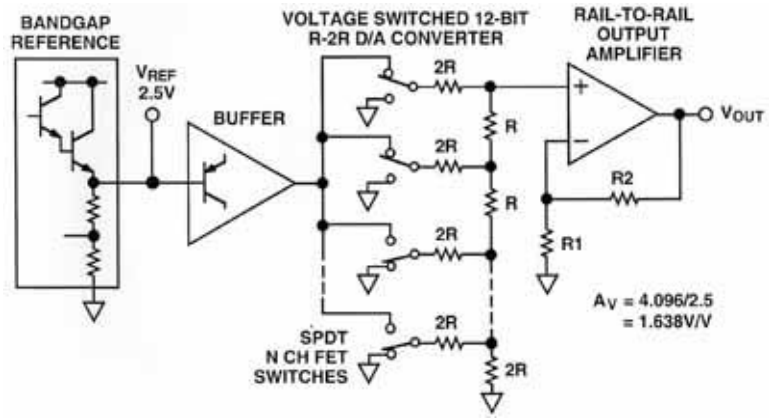



**Figure 6.36**

The other concept which has not been discussed previously is low-voltage, single supply operation. It is at this point that demultiplexed DAC systems rapidly become impractical. One effect of a low supply voltage is that the value of the least significant bit must be reduced. For single +5V operation, the practical limit on full scale voltage at 12-bits is typically 4.096V . This yields an LSB value of 1mV for a 12-bit DAC, which means that the total SHA error budget, including offset voltage, droop rate and hold step, must not exceed ±500µV in order to limit errors to 1/2 LSB.

Improving the droop rate and hold step errors of a multi-channel SHA is difficult because of the limited size of the on-chip capacitors. As the value of the hold capacitors increase, die size and cost rise rapidly. Adding individual SHAs with external hold capacitors is possible, but rapidly increases the component count. Again, the multi-channel DAC is a superior solution.

Another requirement for single-supply, low voltage operation is rail-to-rail operation. Single-supply bipolar amplifiers, using common-emitter output stages, are limited in some low voltage applications because the saturation voltage of the output transistors limits output voltage swing. The AD8522 employs P-channel and

N-channel MOSFETs (Figure 6.37) to provide wide output voltage swing while operating from a single +5 V supply. The output of this type of stage (at a supply rail) looks like the on-resistance of the P or N-channel FET connected to the rail. Obviously, this on-resistance begins to limit the output swing as the output load current is increased.

**AD8522 RAIL-TO-RAIL OUTPUT PERFORMANCE YIELDS 5mA WITH 60mA SHORT CIRCUIT CURRENT**

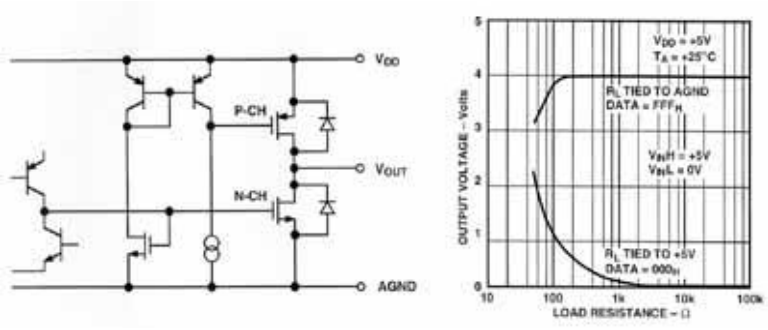



**Figure 6.37**

The effect of a serial interface on pin count is demonstrated by comparing the AD8522 with the similar AD8582. The latter part has a 12-bit parallel interface, and requires 24 pins versus 14 pins for the serial data version.

**AD8582 COMPLETE DUAL 12-BIT SINGLE +5V SUPPLY DAC**

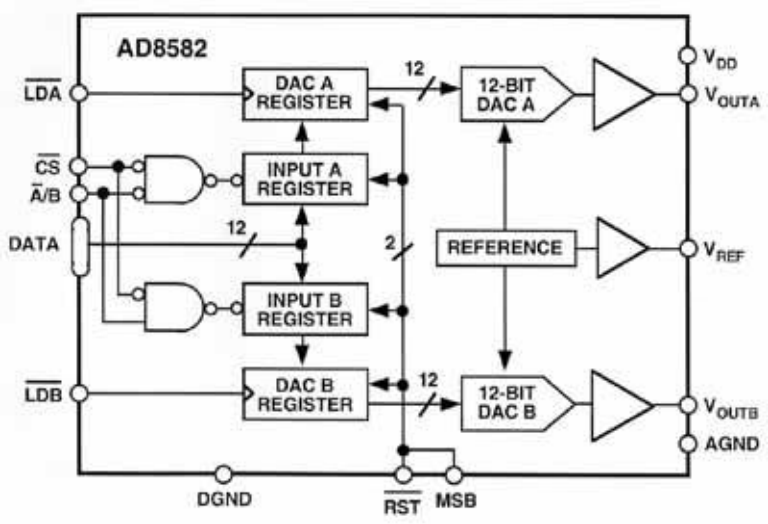



**Figure 6.38**

One significant advantage of the parallel interface is, of course, higher speed. The parallel device can update both 12-bit DACs in 100ns. The serial data version, on the other hand, requires 32 clock cycles to enter the data for two DACs. With a maximum clock frequency of 14MHz, this results in a data update period of 2.2µs.

The parallel-data version also includes complete dual-rank data latches, so that both DACs can be updated simultaneously (Figure 6.39).

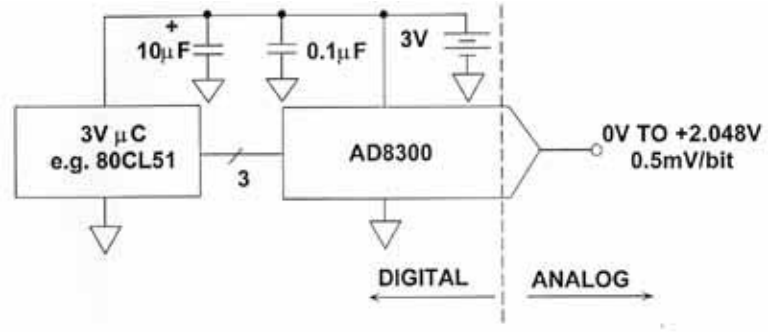
**AD8582 KEY FEATURES**

- **Complete Dual 12-bit DAC**
- **No External Components**
- **Single +5 Operation**
- **1mV/bit with 4.095V Full Scale**
- **True Voltage Output, ±5mA Drive**
- **Parallel Input Register with Fast 30ns Chip Select**
- **Double-Buffered for Simultaneous A and B Output Update**
- **Reset Pin Forces Output to Zero Volts or half Scale, Depending on MSB Pin**
- **Low Power: 5mW**

**Figure 6.39**

The logical extension of a serial data interface and low voltage CMOS technology is expressed in Figure 6.40. While not a multi-channel device, the AD8300 does pack a complete 12-bit voltage output DAC into a single 8-pin package. No external components are required, except for supply bypass capacitors. Since it is capable of operating from a single 3V supply, this device is ideal for battery-powered applications.

**A 12-BIT, +3V DAC SYSTEM BASED ON AD8300**




- No Adjustments or Trimming
- Single-Chip Error Budget Analysis

**Figure 6.40**

The AD8300 has only one analog pin, which is the DAC's voltage output. With only one analog pin, the AD8300 is an ideal device for designers whose experience is mainly digital. All analog circuitry, except for the analog voltage output pin, is transparent to the user. Double-buffered data latches prevent the DAC output from changing while new data is being shifted into the AD8300.

**AD8300 BLOCK DIAGRAM**

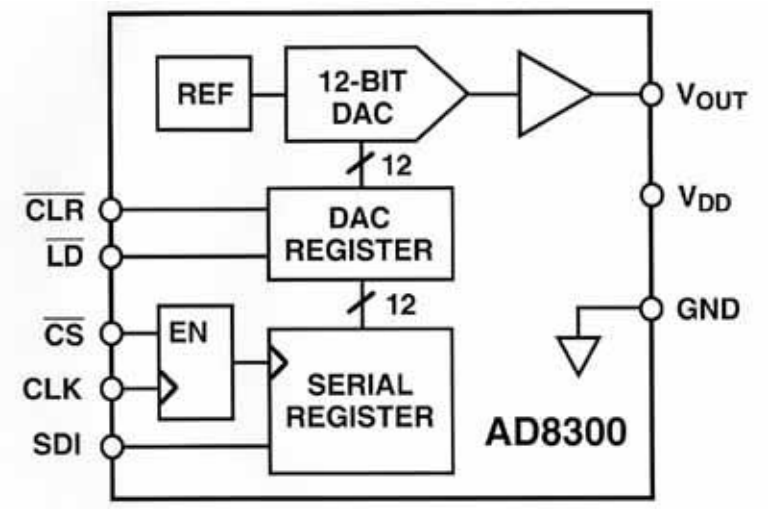



**Figure 6.41**

The AD8300 is laser-trimmed during production, so no calibration or other adjustments are required. The DAC value is simply shifted into the serial data input, and the analog output responds with a pre-trimmed value of:

$$V_{OUT} = D \cdot 0.5mV,$$

where D is a decimal number which represents the DAC input value (that is, 0 to 4095). The full-scale output voltage is 2.0475V, which is appropriate for the minimum supply voltage of 2.7V. The DAC output can be asynchronously set to 0V with the CLR input, if a power-on reset is required.

**KEY FEATURES OF THE AD8300 DAC**

- **Complete Voltage Output 12-bit DAC**
- **Single +3V Operation**
- **No External Components**
- **2.0475V Full Scale Output (0.5mV/bit)**
- **6μs Output Settling Time**
- **Serial Data Input**
- **Asynchronous Clear Input**
- **Low Power; 3.6mW**
- **PCMCIA-Compatible SO-8 Package (1.5mm package height)**

**Figure 6.42**

The data distribution systems discussed so far have illustrated the tradeoffs between demultiplexing a single DAC and using a single chip, multiple-channel DAC. Both of these concepts assume that the system being designed requires several analog voltages in close physical proximity to each other. The design considerations change, however, for systems where different circuit elements are not physically close. Analog signal traces should be kept as short as possible to reduce error sources such as leakage and noise pickup. Digital signals have more noise immunity than analog signals, so the rule of thumb is to locate the DAC as close to its associated analog circuitry as possible.

A complete DAC with serial input can utilize its small size to place the analog voltages near the circuits they control with minimal impact on overall PC board area. Two AD8300s, for example, have a total of only 16 pins. This is only two pins more than the previously-discussed dual-12-bit DAC, yet the two single DACs can be located directly adjacent to subsequent circuits (Figure 6.43). This eliminates long PC board traces (for the analog signal) and reduces noise pickup. Multiple AD8300s can be accessed with one serial data bus, and the outputs of the DACs can change either synchronously or asynchronously.

## REMOTE, MULTI-CHANNEL DATA DISTRIBUTION

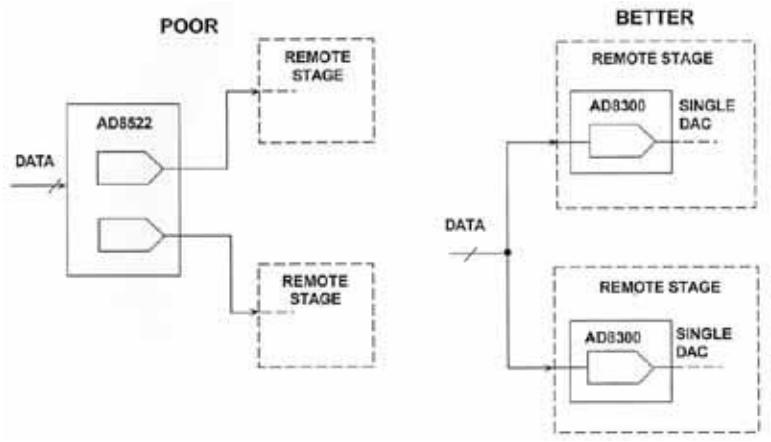



**Figure 6.43**

## REFERENCES


1. **Linear Design Seminar**, Analog Devices, 1995, Chapter 7.

2. **System Applications Guide**, Analog Devices, 1993, Chapter 2.

3. Dan Sheingold, **Analog-Digital Conversion Handbook, Third Edition**, Prentice-Hall, 1986.

4. Adolfo A. Garcia, *Applications of the SMP-04 and the SMP-08/SMP-18, Quad and Octal Sample-and-Hold Amplifiers*, **Application Note AN-204**, Analog Devices, 1991.

5. *A Selection Guide for Serial DACs*, Document Number G1982, Analog Devices, 1994.