Specification for the DECT ARi[1]™ Interface to the Radio Frequency Front End

National Semiconductor
Application Note 908
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INTRODUCTION

This document will describe the I/O necessary to drive the National Semiconductor DECT radio frequency (RF) front end chip set. This is intended to help the system designer define the control signals for the RF front end, implemented as a direct modulation, single conversion receiver architecture. A single conversion transmitter and dual conversion receiver can be added with a second PLL and some other minor changes.

1.0 DECT SYSTEM OVERVIEW

1.1 I/O Requirements

The National Semiconductor solution for the DECT RF front end includes microwave circuits, frequency synthesizers, and pre-baseband functions (modems, DACs, RSSI, etc.). From the block diagram in *Figure 1,* it can be seen that the analog microwave circuits require only a power down signal, but that the digital circuits will require more control signals. The requirements for each part will be described in detail below.

1.2 The Front End Function

The Radio Frequency (RF) Front End serves as the air interface for the communication link. When transmitting, the user transmit data is shaped by the lowpass filter in the baseband processor (LMX2411). This shaped data is then transformed into a modulated waveform by modulating a Voltage Controlled Oscillator (VCO). This modulated signal is amplified to the proper output level by the power amplifier and output through a switch (or circulator), the roofing filter, and the antenna.

When receiving, the signal is input through the antenna, the switch (or circulator), and the roofing filter. The signal is amplified with the low noise amplifier and downconverted with the mixer (LMX2216B) to a fixed intermediate frequency. Channel changes are done by changing the local oscillator frequency driving the mixer with the frequency synthesizer (LMX2320). The intermediate frequency is then stripped of its information by a limiter/discriminator (LMX2240). Data values are then recovered from the signal (LMX2411) and sent to the burst mode controller. The received signal strength is also recovered (LMX2240) and filtered. The RSSI signal is digitized by an ADC on the burst mode controller or on the microprocessor.

To accomplish modulation of the VCO, the phase-locked loop that is used to set the channel frequency must be opened. This is done by powering down the LMX2320 PLL using the Power Down (PD) pin. When this is done, the charge pump output shifts to a TRI-STATE® mode, effectively preserving the loop voltage. The modulating signal is then added to the loop voltage by a resistive adder. The DECT TDMA/TDD bursts are short enough that with appropriate components and careful design, the discharge of the loop filter voltage (frequency accuracy) is within DECT specifications. Note that this method only requires a VCO to have a single tuning port.

A critical feature of open loop modulation is control over the VCO load. The receive power down signal turns the receive mixer on and off, changing its impedance. The LO switch transitions from this mixer to the power amplifier input. The power amplifier input impedance is a function of the power amplifier power down signal and of input power to it. The timing and sequence of these control signals will affect the VCO frequency error (jump) and should be carefully managed once the PA, switch, mixer, and VCO are chosen. See Section 2.5 for more details on open loop modulation.

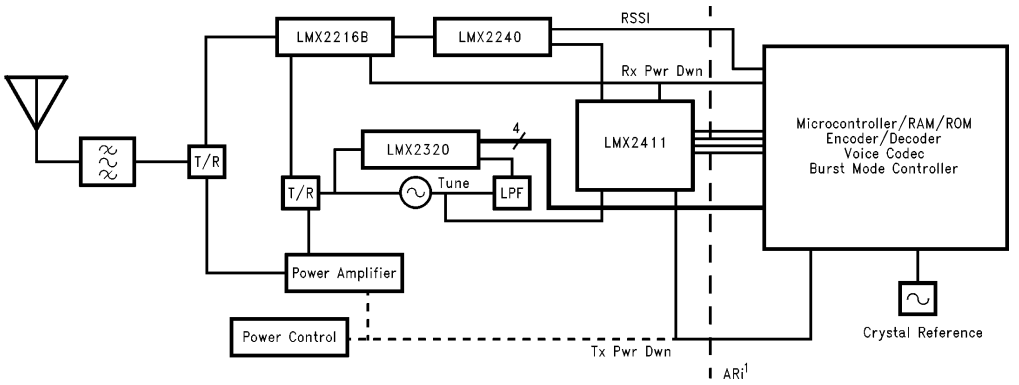

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FIGURE 1. Typical DECT RF Front-End Subsystem with ARi[1] Dividing Line Indicated

2.0 SYSTEM CONTROL SIGNAL REQUIREMENTS

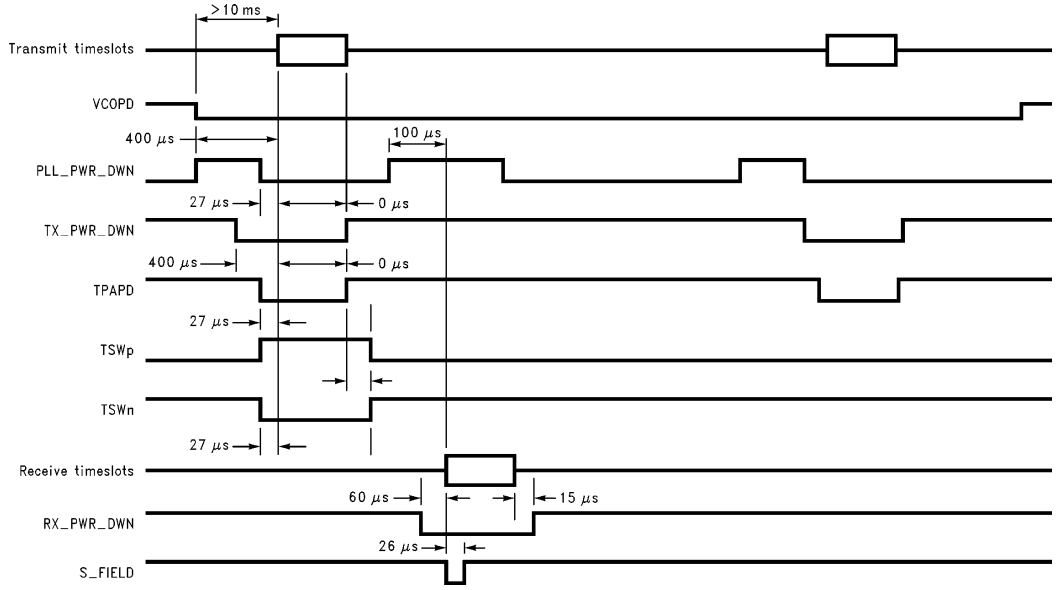

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FIGURE 2. A Typical Timing Diagram for the RF Front End Power Down Signals (during Active Locked Mode).

Symbol	Parameter	Time before Burst			Time after Burst			Unit
		Min	Typ	Max	Min	Typ	Max	
VCOPD	VCO Power Down	10						ms
PLL__PWR__DWN	PLL Power Down HIGH	30	150	400				µs
TPAPD	Power Amplifier Power Down	15	27	40	0			µs
TX__PWR__DWN	Transmit Section Power Down	30	50	240	0			µs
TSWp	T/R Switch Positive Signal	15	27	40		27		µs
TSWn	T/R Switch Negative Signal	15	27	40		27		µs
RX__PWR__DWN	Receiver Section Power Down		60			15		µs
S__FIELD	DC Compensation Circuit Enable		0					µs

In *Figure 2* above, the timing diagram for the overall front end power down signals is shown. Note that this is a typical case, and that in fact there are some signals that will vary in length. The table below shows the ranges of values for the various power down signals. In the table, the times are referenced to either the time required before a burst (timeslot) starts or the time required after a burst ends.

In the above table and in *Figure 2,* it can be noticed that the VCO is turned on and left on for the entire active locked period, while the PLL is powered down between bursts. The transmit and receive power down signals, as well as the switch signals (see Section 2.3), are toggled for each burst to conserve current. The numbers given in the table and *Figure 2* represent a typical DECT application. The power amplifier should be ramped both on and off in 27 µs each (DECT specification, Part 2: Physical Layer, Sections 5.2–5.3, *Figure 13*). The S__FIELD signal should be enabled at the start of the burst and last for 30 bits of the 32-bit preamble. This allows for some timing offsets in the burst mode logic. The transmit/receive switches need to be thrown at the same time or before the power amplifier begins its final power up, so their times are chosen to be the same before the burst, but they are delayed while the power amplifier turns off to avoid any more amplitude modulation of the signal than necessary and to correctly terminate the power amplifier. The phase locked loop and the transmit section must be turned on 400 µs before PLL__PWR__DWN goes LOW so that the loop compensates for the mid band voltage of the modulating signal. This is why they have two different power down signals offset in *Figure 2.* In transmit mode, the PLL must first settle to the transmit frequency and then be opened to allow modulation to take place. The transmit DAC's output should be at mid-range voltage prior to opening the loop to ensure that the loop centers on the correct frequency and then deviates equally to each side based on the modulation (see *Figure 3*). This is achieved by toggling Tx PD LOW (i.e., powering up the transmit portion) on the LMX2411 and holding Tx Data constant (either HIGH or LOW). The first edge on Tx Data will synchronize the LMX2411 to the transmit data and will also start transmission of the data through the digital filter.

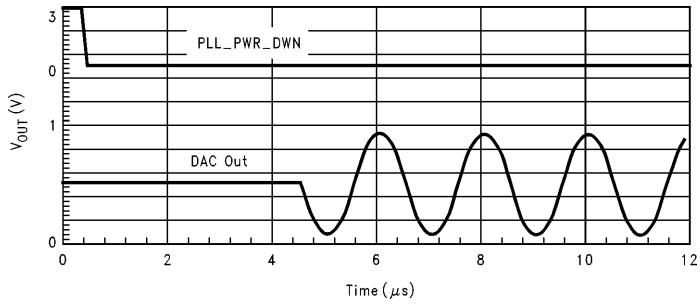

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FIGURE 3. Plot of PLL__PWR__DWN Signal and Modulator Output after TX__PWR__DWN is LOW

The receiver must be powered up 60 μs before a receive burst to allow the receive chain to fully power up and settle. Note that some standard products, such as the Sierra Semiconductor SC14400, have burst mode control signals that comply with the ARi[1]. The SC14400, for example, provides 9 pins for power down and load enable functions that are fully flexible with respect to timing. These signals can switch at any bit time, as long as only one is switched at a time. Also, two of these pins are higher in current to support the current required for PIN diode switches. A typical order of power down signals for one burst is the following:

Action:

1) Program PLL to the transmit frequency
2) Turn on PLL
3) Turn on Baseband Processor transmit section
4) Throw LO switch to ''Transmit'' position
5) After loop settles, open PLL
6) Throw RF output switch (if any) to ''Transmit'' position
7) Ramp on power amplifier
8) Transmit data
9) Ramp off power amplifier
10) Throw Transmit/Receive switches to ''Receive'' position
11) Turn off Baseband Processor transmit section
12) PAUSE
13) Program PLL to the receive frequency
14) Turn on PLL
15) Turn on receiver section
16) Receive data; generate S__FIELD signal for DC compensation
17) Turn off receiver section
18) Turn off PLL
19) Repeat steps 13) through 18) to monitor a second channel.

It is interesting to note that the unlocked output from the synthesizer is very low in noise. The user should consider using the unlocked LO during receive mode. This would result in a lower noise LO, but it could also result in more frequency drift. The drift specification in DECT is 13 kHz/ms. Presently, National Semiconductor has observed typical drift measurements of 55 kHz/second, or 55 Hz/ms.

2.1 The Receive Chain

The LMX2216B is the Low Noise Amplifier and Mixer, and the LMX2240 is the Intermediate Frequency Receiver. For DECT, these functions should be active only during receive mode. To accomplish this, the power down pin of either part should be driven low to activate the device and high to power it down. This polarity is chosen so that the user can simply ground the power down pin to permanently activate the part. The power down signal for each part should be the global receive power down (RX__PWR__DWN) signal for the entire receiver. This and all global power down signals should be CMOS power down signals unless noted otherwise. Using CMOS signals and CMOS power down switches on board each IC reduces power consumption and avoids the longer power up times that would be governed by decoupling capacitors on regulated supplies.

In addition to the power down signal, the analog output of the LMX2240's RSSI circuit should be sent to either the burst mode controller (e.g., Sierra SC14400) or to the microcontroller (e.g., Mitsubishi M37702) for digitization and peak hold by the ADC. Note that the microcontroller's ADC may not be fast enough to do the peak hold function digitally. In that case, an analog peak hold circuit must be added before the input to the microcontroller's ADC.

2.2 The Phase Locked Loop (PLL) Frequency Synthesizer

The LMX2320 is the 2.0 GHz frequency synthesizer. This part is provided with a power down pin as well as three pins to be used for serial programming of the desired center frequency and step size. The power down pin requires a separate control signal (PLL__PWR__DWN) because the synthesizer may be operating during both transmit and receive modes. The programming interface is a three wire MICROWIRE™-compatible interface with write-only capability. The Load Enable (LE) pin is active low. When the LE pin goes high, the loaded data is sent to the appropriate register in the synthesizer.

The timing for the LMX2320 is as follows. When the LE pin is low, the LMX2320 is ready for data from the channel controller (microprocessor or burst mode controller). On each rising edge of the clock, a serial bit is loaded from the data input. When LE goes high, the data is loaded into the prescaler and reference registers, and the channel is changed. The data cannot be shifted into the shift register until LE goes low.

The LMX2320 has two registers that need to be programmed. The Reference divider (R Counter) is a counter that divides the (crystal) reference frequency. It is programmed with a 14-bit word when the control bit is high, or ''1''. A fifteenth bit is used to set the programmable (128/129 or 64/65) prescaler. The frequency divider (N Counter) divides the input frequency and is programmed with a 18-bit word when the control bit is a low, or ''0''. The structure of the words is given on the following page.

To program the R Counter, the data should be the following (P = ''1'' for 64/65, P = ''0'' for 128/129):

P	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	C
d*	d	d	d	d	d	d	d	d	d	d	d	d	d	d	1

*d signifies a desired data bit, i.e., a ''1'' or a ''0''

To program the N Counter, the data should be the following:

D_{17}	D_{16}	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	C
d*	d	d	d	d	d	d	d	d	d	d	d	d	d	d	d	d	d	0

*d signifies a desired data bit, i.e., a ''1'' or a ''0''

For DECT operation using a 10.368 MHz crystal and a reference, or step size, of 1.728 MHz,

R = 6

N = 1089 . . . 1098

P = 64

For further information, please consult the LMX2320 Data Sheet.

2.3 The Voltage Controlled Oscillator (VCO) and Transmit/Receive (T/R) Switches

The VCO power down signal will probably originate from the LP2951 regulator directly. When the regulator is powered up, the VCO will be powered up. This is due largely to the long turn on times for VCO's. The VCO's individual data sheets must be consulted for turn on time, as these may vary among manufacturers.

Up to two switch functions are required. The first is the signal control between the antenna and the Low Noise Amplifier (LNA) or power amplifier. A quarter wave length pin diode switch directs the RF signal to the LNA with low power dissipation. In transmit mode, current is passed through two PIN diodes to provide a low loss connection from the power amplifier to the antenna, and to isolate the LNA. Note that this switch can be replaced by a circulator.

The second switch controls the output of the VCO. This switch directs the VCO output to the receiver mixer or directly to the power amplifier input. *Figure 4* shows these functions below. Presently, two VCO manufacturers, ALPS and muRata, produce wideband VCOs which span the entire 130 MHz needed to achieve a single conversion receiver.

2.4 The Power Amplifier

The power amplifier requires a separate TPAPD signal for turning the PA on because of the power amplifier ramping required by DECT. (TX__PWR__DWN must turn on earlier to allow the PLL to lock to the correct frequency and not be offset by the mid band voltage of the LMX2411.) The power amplifier can be ramped with a single RC circuit or with a more complex raised cosine shaping. The technique used will depend on the power amplifier manufacturer's circuit. One circuit which has been used at National for GaAs power amplifiers is shown in *Figure 5.*

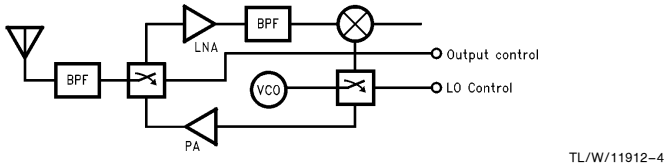

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FIGURE 4. Block Diagram of the Possible Switches Necessary in the RF Front End

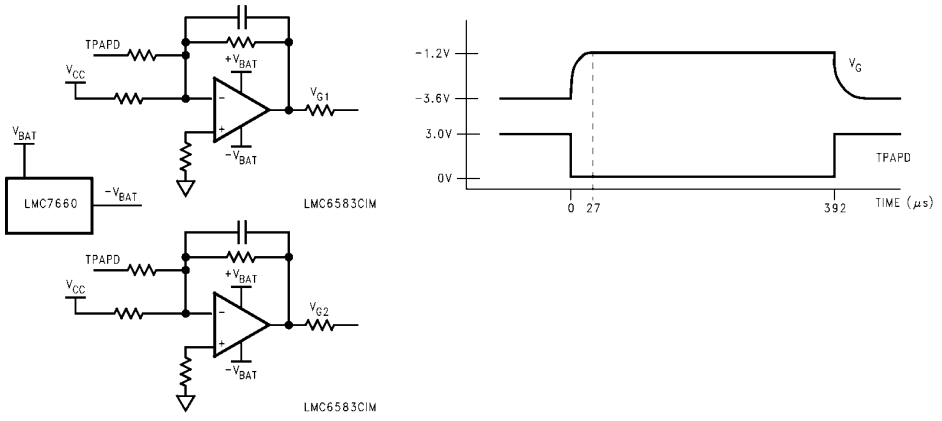

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FIGURE 5. The Circuit for the Power Amplifier Ramping Used by National Semiconductor and its Typical Performance

2.5 The Baseband Processor

2.5.1 General Functions

The LMX2411 is the baseband processor, or the interface between the RF front end and the digital back end. It functions in both the transmit mode and the receive mode, although only part of the chip is powered up at any given time. The LMX2411 has two power down pins, Tx PD and Rx PD, that should be driven with the appropriate global power down signal. This power down configuration reduces current consumption. In addition to the power down pins, the LMX2411 requires a Sys Clock and Tx Data input, a control signal input for its DC compensation circuit ($\overline{\text{S-Field}}$), and a Comp Out output line.

The Sys Clk input can be one of three system clocks commonly used in DECT: 10.368 MHz (9x), 13.824 MHz (12x), and 18.432 MHz (16x). This clock is used to clock the ROM filter and shift the Tx Data bits through the ROM addresses. Tx Data is the actual information data to be transmitted and is input from the burst mode controller. The control line that is needed for the DC compensation circuit, S__FIELD, also comes from the burst mode controller. This should only enable the DC compensation circuit during 30 bits of the DECT preamble to allow for 3 bits of timing inaccuracy. The DC compensation on the LMX2411 is an analog loop using a sample and hold circuit. The DC compensation method using the sample and hold circuit is intended to provide a fast RC averaging over a known sequence (DECT preamble). The analog method can be used without an S__FIELD signal, providing a long term average of the DC value through the use of a large capacitor on pin 2 of the LMX2411. However, this technique is not recommended due to its long start-up time and its sensitivity to long strings of 1's and 0's. Note that some burst mode controllers, in particular the Sierra SC14400, can support both this method and a digital DC compensation loop (see *DC Compensation*). The only output of the LMX2411 is the comparator output, which provides a CMOS level output ready for timing recovery to the digital back end.

2.5.2 Open Loop Modulation

Open loop modulation is a technique that allows for a relatively simple implementation as long as frequency pushing and load pulling effects can be controlled. The loop is opened by powering down the PLL, which in the LMX2320 results in a TRI-STATE at the charge pump output. For short bursts, the loop filter will not lose the charge, and the center frequency will not drift. *Figure 6* shows a sample circuit for modulating on an open loop. Note that the VCO requires only one tuning port for both locking and modulation. R_1 and R_2 will vary depending on which wideband VCO is used. The proper equation to be used in determining R_1 and R_2 is below:

$$V_{DAC} * \frac{R_2}{R_1 + R_2} * K_V = 576 \text{ kHz} \quad (1)$$

In this case, K_V is the VCO sensitivity, expressed in MHz/V, and V_{DAC} is nominally 1V. Generally, R_1 will be on the order of 50 kΩ to 250 kΩ, and the ratio of R_1 to R_2 will vary from 30:1 to 50:1 for wideband VCOs, and will be smaller for narrowband VCOs. Also, the 576 kHz is the peak-to-peak frequency deviation for DECT, which means the peak frequency deviation is half of that, or 288 kHz.

It should be noted that the schematic in *Figure 6* contains a unity gain buffer op amp at the output of the PLL's loop filter. This op amp must have a low output impedance so as not to affect the voltage summing node for open loop modulation. This op amp will be necessary when using VCO's with high varactor leakage to prevent the varactor from discharging the loop capacitor and therefore causing frequency drift. This buffer should be powered up whenever the VCO is powered up, and so should be connected to the VCO's power down line. *Figure 7* shows a plot of typical frequency jump and drift that can be expected from open loop modulation when the load pulling and frequency pushing effects have been properly controlled.

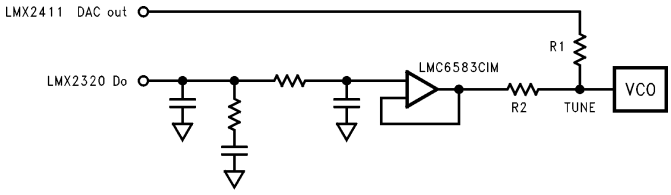

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FIGURE 6. Circuit Diagram for Direct, Open Loop Modulation

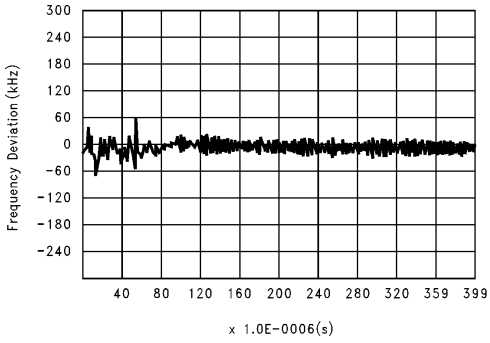

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FIGURE 7. Plot of Frequency Discriminator Output of Unmodulated Open Loop Carrier over a 400 μs Burst Showing the Loop Opening at 60 μs and the Resulting (Lack of) Drift. Units are kHz/μs.

Frequency pushing is controlled by putting a series 10Ω resistor and a shunt 1 μF to 4 μF capacitor on the VCO V_{CC} line from the LP2951 voltage regulator. Load pulling is controlled by using an attenuator and an RF buffer between the VCO and the power amplifier. The power amplifier and T/R switch both affect load pulling. RF coupling can also cause frequency drift, and this is controlled by providing good shielding between the power amplifier and the VCO.

2.5.3 DC Compensation

Compensation of the drift in DC of the demodulated eye due to frequency error, co-channel interference, or temperature effects can be implemented by using an analog "sample and hold" technique, or by using a digital duty cycle detection. In the analog method, the received, demodulated signal is input both to the comparator "+" input and to the sample-and-hold (S&H) buffer amplifier. The S&H buffer allows a single RC filter to average the DC value of the received signal without distorting it. This DC value is connected to the "−" input of the comparator. When the signal S__FIELD is used (named after the synchronization field in DECT), this circuit can acquire the DC voltage during the preamble and then hold it (with the external capacitor) for the duration of the burst. This solution avoids the problem of long strings of 1's and 0's that conventional continuous averaging circuits have while still reacting quickly to acquire the proper DC average at the beginning of a burst. This solution is provided internally to the LMX2411. *Figure 8* shows a typical response curve of the DC threshold level from initial startup. Note that the discharge of the capacitor is very low, which means that once the first burst acquisition has been done, all following bursts should be recovered with minimal CRC errors.

Another method of DC compensation is to monitor the duty cycle of the output of Comp Out, and adjust the level of an external threshold DAC that drives the LMX2411's comparator threshold directly. The digital method has the added advantage that the last value of the DAC can be pre-loaded for each timeslot, thus introducing memory into the system. The Sierra SC14400 supports both DC compensation methods.

2.6 Summary of ARi[1] Signals

The following is a summary of all thirteen (13) signals that are contained in the ARi[1] specification and their descriptions.

2.6.1 Tx Interface

2.6.1.1 TX__PWR__DWN

This signal is used to change the transmitter between power down and active modes. TX__PWR__DWN should go low 460 bits (400 μs) prior to start of transmission.

2.6.1.2 TPAPD

This signal is used for turning the power amplifier on and off. This signal should enable the power amplifier 31 bits (27 μs) prior to start of transmission.

2.6.1.3 TSWp/TSWn

These signals are used for the Tx/Rx switch at the antenna and/or VCO output. They are inverse signals of each other, and one or both may be used in a given implementation. In the case of TSWp, a "LOW" signal indicates the output of the VCO goes to the Rx mixer. A "HIGH" signal indicates the output of the VCO goes to the power amplifier. For TSWn, the polarity is reversed. This signal should switch approximately 30 bits (27 μs) before the start of either transmission or reception of the signal.

2.6.1.4 TX__DATA

Data to be transmitted. This is sent three bit times prior to start of transmission to account for three bit delay in the ROM filter. Also, three padding bits are added at the end of the burst to ensure the last desired bit is transmitted. The polarity of this signal determines reset state of LMX2411 ROM address. See the LMX2411 data sheet for more details.

2.6.1.5 SYS__CLK

This is the reference clock for both the LMX2411 and the LMX2320. It should have a frequency of either 10.368 MHz, 13.824 MHz, or 18.432 MHz and should be active anytime the transmitter or frequency synthesizer is active. This signal can be a CMOS signal or have a voltage swing with as little as 500 mV_{PP}.

2.6.2 Rx Interface

2.6.2.1 RX__PWR__DWN

This signal is used for the Rx to change between power down and active modes. RX__PWR__DWN should go LOW 70 bits (60 μs) prior to start of reception of the signal.

2.6.2.2 RSSI

This is the analog RSSI signal that originates from the LMX2240. This signal should be connected to an ADC that is either in the burst mode logic or the microcontroller.

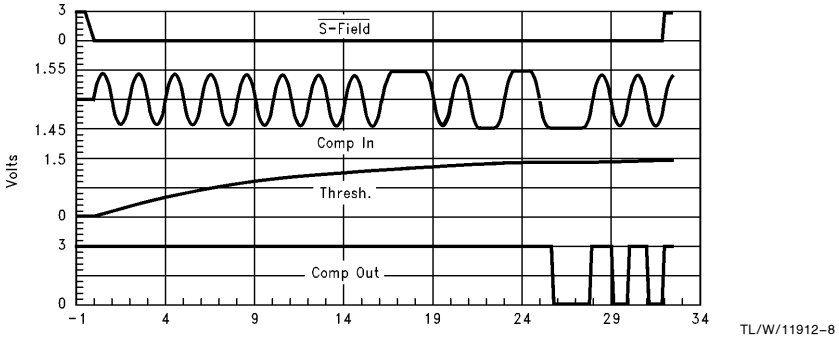


FIGURE 8. Plot of DC Compensation Circuit Response vs Time from Full Discharge of Hold Capacitor

2.6.2.3 RX__DATA

Demodulated, received data for input to the burst mode controller. This is the output from the comparator.

2.6.2.4 S__FIELD

This signal is used to enable the analog DC compensation circuit on the LMX2411. This signal should go LOW 2 bits (2 μs) to 0 bits (0 μs) before the start of reception of the signal. This signal should go HIGH 32 bits (29 μs) to 30 bits (27 μs) later for an effective 30-bit averaging period for the sample and hold circuit.

2.6.3 Synthesizer Interface

2.6.3.1 PLL__PWR__DWN

This signal changes the phase-locked loop (PLL) frequency synthesizer between power down and active modes. PLL__PWR__DWN should go HIGH between 115 bits (100 μs) and 461 bits (400 μs) before the PLL will be locked. **Note that this results in a blind slot implementation for DECT.** PLL__PWR__DWN should go LOW 31 bits (27 us) before the start of a transmission to unlock the PLL. **NOTE: THE LMX2320 PLL CAN BE PROGRAMMED IN THE POWER DOWN STATE.**

2.6.3.2 ENABLE

Enable signal for the LMX2320 programming interface.

2.6.3.3 DATA

Data line for the LMX2320 programming interface.

2.6.3.4 CLOCK

Clock line for the LMX2320 programming interface.

2.6.4 System Signals

2.6.4.1 VCO__PD

May be used as a system PD as well by connecting to an LP2951 (or equivalent) voltage regulator output. To power down the VCO, the regulator would be turned off, which would also turn off the entire RF front end.

2.6.4.2 V_{BAT}

The battery voltage that presumably will come from 3 NiCad battery cells or their equivalents. This is the power supply that is regulated on board the RF front end. All ICs are driven by this except the power amplifier, which operates directly from the battery. This signal should be connected directly to the battery with short lead lengths to minimize losses during times when the power amplifier is on and also to avoid lead inductances which cause variations in V_{CC} and V_{BAT}.

2.6.4.3 GND

This is the return path to the battery.

3.0 ELECTRICAL SPECIFICATIONS

The RF front end runs on a single +3V supply. The table below gives the pertinent electrical specifications to interface to the RF front end's CMOS circuitry.

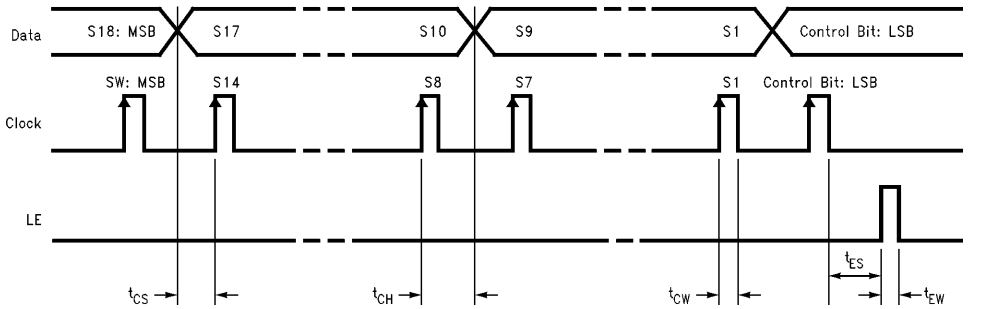
ELECTRICAL CHARACTERISTICS

(The following specifications apply for supply voltage V_{CC} = +3V ±5% V unless otherwise specified).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DIGITAL INTERFACE SECTION						
V_{OH}	High-Level Output Voltage	I_{OH} = −1.0 mA	V_{CC} −0.4			V
V_{OL}	Low-Level Output Voltage	I_{OL} = 1.0 mA			0.4	V
V_{IH}	High-Level Input Voltage		V_{CC} − 0.8			V
V_{IL}	Low-Level Input Voltage				0.8	V
I_{IN}	Input Current	GND < V_{IN} < V_{CC}	−1.0		1.0	μA
t_{CS}	Data to Clock Setup Time	See Data Input Timing	50			ns
t_{CH}	Data to Clock Hold Time	See Data Input Timing	0			ns
t_{CWH}	Clock Pulse Width High	See Data Input Timing	50			ns
t_{CWL}	Clock Pulse Width Low	See Data Input Timing	50			ns
t_{ES}	Clock to Enable Setup Time	See Data Input Timing	50			ns
t_{EW}	Enable Pulse Width	See Data Input Timing	50			ns

Note 1: DC Electrical Characteristics for the digital section apply to all digital input and output pins. This includes Clock, Data, LE, PD, Tx Data, Tx PD, Rx PD, Comp Out and $\overline{\text{S-Field}}$.

SERIAL DATA INPUT TIMING



TL/W/11912–9

NOTES: Parenthesis data indicates programmable reference divider data.
Data shifted into register on clock rising edge.

LIFE SUPPORT POLICY

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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