Analysis and Design of a Frequency-Hopped Spread-Spectrum Transceiver for Wireless Personal Communications

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***Abstract*—Personal Communications Services (PCS) require low-power radio technologies. One such transceiver architecture employing frequency-hopped spread-spectrum techniques is presented. System features such as antenna diversity with equal-gain combining and sequential hop combining are incorporated into the transceiver design to achieve robust wireless digital data transmission over fading channels. A direct-conversion architecture from radio frequency (RF) to baseband reduces the overall power consumption by eliminating intermediate frequency (IF) components. High-rate frequency hopping with frequency-shift keying (FSK) modulation is implemented using a direct digital frequency synthesis technique. A multiplierless correlation FSK detector, suitable for direct-conversion receivers, has been designed for quadrature noncoherent detection. Robust acquisition algorithms based on energy detection and pattern matching and tracking architectures using digital phase-locked loops are also described for system synchronization. The proposed transceiver is well-suited for low-power PCS applications and other portable wireless communications.**

***Index Terms*—Frequency hop communication, frequency shift keying, radio receivers, spread-spectrum communication, synchronization, tracking loops, tranceivers.**

I. Introduction

RECENT advances in digital communications, advanced signal processing, and very-large-scale integrated circuit (VLSI) technologies have all contributed to explosive growth in personal communications. Low-power radio access technology is one of the key technical challenges for universal personal communications. The objective of this paper is to describe such a low-power, handheld, robust communications transceiver using frequency-hopped spread-spectrum (FH/SS) techniques. In the proposed transceiver, low power and robustness are emphasized and optimized at all levels of the transceiver design hierarchy: system, architecture, and logic (circuits). An all-CMOS implementation of the transceiver has been developed to demonstrate a communication link in the 902–928 MHz ISM band [1]. It will support data rates up to 160 kbps, which is the standard narrowband Integrated Services Digital Network (ISDN) rate. Section II briefly deals with the system issues and the rationale behind the low-power transceiver. In Section III, the transceiver architecture is described including both RF and baseband components. Detailed baseband processing block descriptions are also given in Section IV. Section V discusses the implementation of robust synchronization algorithms and architectures for master–slave configured frequency-hopped radios. Finally, concluding remarks are made in Section VI.

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II. System Background

The key advantages of the DS technique applied to digital cellular systems, such as universal one-cell frequency reuse, soft handoff, voice activity utilization, and no need for frequency planning, are well-documented in recent papers [2], [3]. However, the FH technique also provides some unique advantages, especially for PCS radios where low power and robustness are two key elements. To achieve significant processing gain or frequency selectivity in a spread-spectrum system, the total spread bandwidth should typically be wider than the coherence bandwidth. In a DS-CDMA system, this requires a rather broadband radio. For an FH system, however, the signal spectrum behaves like a narrowband system at each hop. The signal processing is performed at the hop rate, which is much lower than the chip rate encountered either in a DS-CDMA or TDMA system. This potentially results in much lower portable power consumption. Furthermore, the synchronization requirements in an FH system are not as stringent as in a DS system.

Dual antenna diversity is incorporated into the transceiver design to mitigate multipath fading which is one of the most serious impairments encountered in the radio channel. FH systems also have the advantage of resisting multipath fading by sending many signals at different frequencies. Due to redundancy, if some of these signals are corrupted by interference or fading, the receiver is still able to recover the correct information by using a (sequential) hop combining receiver [4]. The proposed transceiver is a slow frequency hopping (SFH) system, meaning the hop rate is slower than the symbol rate. It should be noted, though, that our system still requires a high hop rate. There are many fundamental differences in the transceiver design and implementation between a very low hop rate SFH-TDMA system, which hops to a new frequency every frame (i.e., hop rate $\cong 50$ Hz), and the proposed SFH-CDMA transceiver. It hops every eight symbols, which results in a hop rate of 20 kHz at a symbol rate of 80 kHz. This mandates the implementation of a fast hopping synthesizer. However, fast hopping typically requires a noncoherent detection scheme because the signal loses phase continuity whenever it hops to a new frequency. This implies an

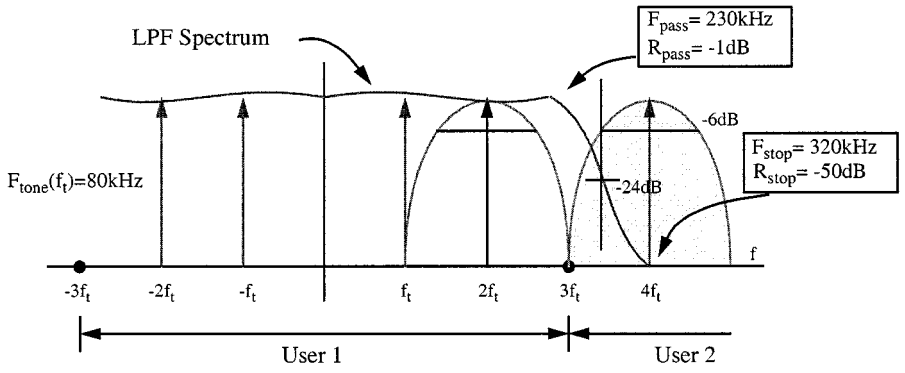


Fig. 1. Proposed quaternary FSK tone assignment.

SNR versus BER performance penalty (e.g., about 6 dB compared to coherent PSK) [5]. However, the combination of frequency diversity, reduced hardware complexity, and low power dissipation partially compensates for this penalty and thus justifies this choice for low-power handheld devices.

The proper choice of the duplexing scheme impacts both the system design and the radio implementation [6]. To allow simultaneous bidirectional communications, an FDD system requires two separate local oscillators, one for the transmitter and the other for the receiver. In a TDD system, one local oscillator can be time-shared between transmit and receive frames. An expensive (in cost and size) frequency duplexer is also required in an FDD system which uses the same antenna for bidirectional transmission. TDD, however, does not require a duplexer. A simple RF switch or equivalent isolates transmit and receive signals from each other in time. For future miniaturized PCS portables, size could be a limiting factor; therefore, TDD is more favorable. In addition, TDD is essential to avoid self-interference seen by the antenna when both uplink and downlink share the same band as in Digital European Cordless Telecommunications (DECT) and our frequency-hopped CDMA system.

Noncoherent FSK modulation is quite suitable for an FH system. Actually, FH can be thought of as an extension of FSK where tone frequencies are not fixed. An FSK radio with FH transmits an RF frequency which is a combination of a tone frequency, a hop frequency, and a fixed carrier frequency

$$F_{rf} = F_{\text{carrier}} + F_{\text{hop}} + F_{\text{tone}}. \tag{1}$$

Hop and tone frequencies can easily be generated using a direct digital frequency synthesizer (DDFS), while the fixed carrier frequency can be produced by a voltage controlled oscillator within a phase-locked loop. For the proposed architecture, quaternary FSK signaling is chosen since it has a 33% better efficiency than binary FSK for multi-user scenarios where a guard band is required between each user channel. One complete tone spacing is skipped between user channels to provide the minimum guard band (Fig. 1). Tones near dc, however, are separated by two times the minimum tone spacing because the smallest tone must be located at $\pm F_{\text{tone}}$, not at $\pm F_{\text{tone}}/2$, for the chosen early–late phase detection scheme of the clock recovery loop to work properly [7]. This guarantees the orthogonality property to hold over half of the symbol time (refer to Section V-C).

TABLE I
FH/SS TRANSCEIVER SPECIFICATIONS

Multiple Access Scheme	Frequency-Hopped CDMA
Modulation Scheme	Quaternary/Binary FSK
Duplexing Mode	Time Division Duplex
Channel Coding	Convol. Code (R=1/2, K=6)
Hopping Bandwidth	26 MHz (902-928 MHz)
Max. Data Rate	160 kbit/s
Symbol Rate	80 kHz
Frequency Hop Rate	20 kHz (1 hop per 8 symbols)
Antenna Diversity	2 with separate rx channels
Maximum Range	500 meters
Transmission Power	20 μW - 20 mW

III. TRANSCEIVER ARCHIECTURE

A. Overall Architecture

The proposed frequency-hopped transceiver, whose specifications are summarized in Table I, employs direct conversion, single sideband (SSB) modulation, hard-limiting, and quadrature demodulation (Fig. 2). A direct-conversion architecture, also known as homodyne, converts the signal from RF directly to baseband or vice versa, with no IF. This eliminates image-reject filters and other IF components, thereby making high levels of integration possible. Our prototype transceiver integrates all RF and baseband processing components into a monolithic CMOS solution [8]. This enables low power dissipation, smaller size, and low cost to be achieved.

One of the most critical components of a frequency- hopped transceiver is a low-power hopping synthesizer. Conventional hopping synthesizers use analog phase-locked loop techniques. The analog PLL-based synthesizer has programmable frequency dividers in the loop to generate different frequencies. The hopping speed of the analog synthesizer is thus limited by the settling time of the loop. Typical settling times of these analog hopping synthesizers are on the order of few hundreds of microseconds [9]. A direct digital frequency synthesis (DDFS) technique combined with a digital-to-analog converter (DAC) provides an alternative way to implement a fast frequency-agile synthesizer. Samples of a sine wave are generated directly from the sine ROM which is addressed by the output of a digital phase accumulator. The DDFS approach has several key

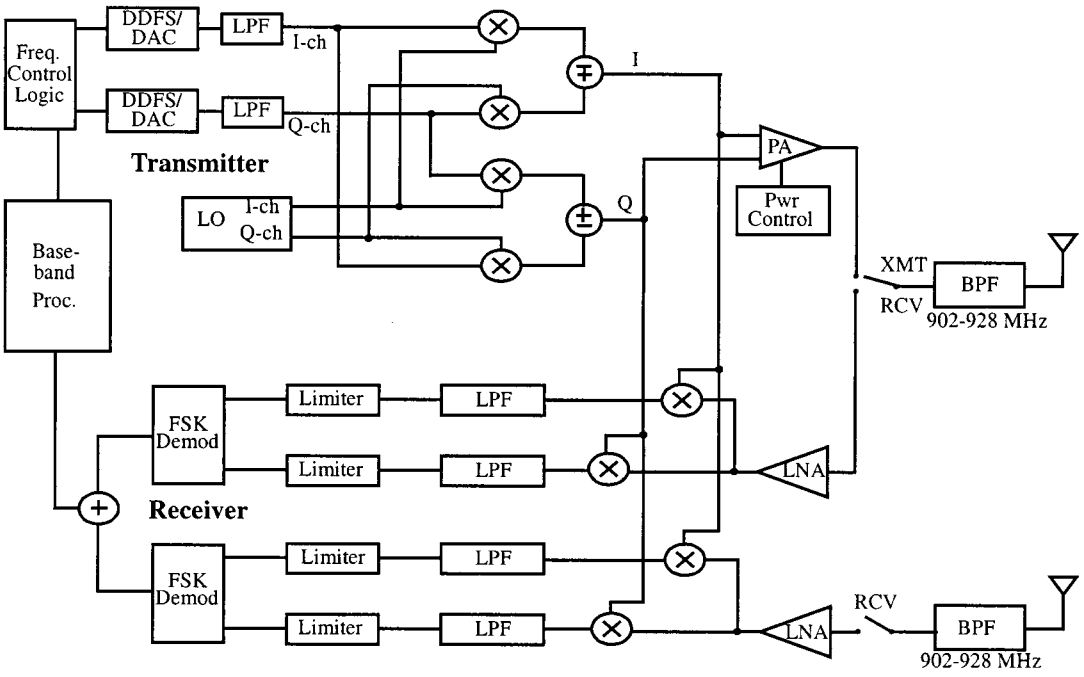


Fig. 2. Overall FH/SS transceiver architecture.

advantages over conventional analog PLL-based synthesizers, the most important of which is being able to achieve rapid frequency changes with continuous phase. The hop rate is no longer limited by the RF synthesizer settling time but by the system requirements.

The detailed RF architecture description is beyond the scope of this paper, and thus only functional descriptions of the RF architecture are briefly mentioned here. When a baseband FSK signal is upconverted to RF without using the SSB technique, it will produce both the desired frequency and its image symmetric around the carrier frequency. A very narrow bandpass filter can remove the unnecessary image. However, the task of building a narrow bandpass filter at high frequency is not an easy problem, especially when an on-chip filter is required for monolithic integration. The SSB technique provides an effective way to suppress the image signal without resorting to bandpass filters with sharp roll-off. The function of the SSB modulation can mathematically be explained using complex-signal representations

$$\begin{aligned} I_{\mathrm{USB}}(t) &= \mathrm{Re}\{\exp(j2\pi f_c t)\cdot\exp(j2\pi f_x t)\} \\ &= \cos[2\pi(f_c+f_x)t] \qquad (2) \\ I_{\mathrm{LSB}}(t) &= \mathrm{Re}\{\exp(j2\pi f_c t)\cdot\exp(-j2\pi f_x t)\} \\ &= \cos[2\pi(f_c-f_x)t]. \qquad (3) \end{aligned}$$

Equations (2) and (3) convey two important properties of the SSB modulation, both employed in our transceiver architecture. The first is that only one desired tone is produced by taking the real part of the multiplication of two complex signals which requires two real multipliers followed by a summing node. Secondly, the choice of the sign of f_x, which is controlled digitally by the input frequency control word of the DDFS, determines whether the generated signal will be either upper sideband (USB) or low sideband (LSB) with respect to the carrier frequency. This suggests that a quadrature digital synthesizer which spans only half the required band (13 MHz) can effectively achieve the total 26 MHz of hopping bandwidth using this sign technique. In fact, this is one of the key factors that were exploited to implement the low power digital hopping synthesizer [10]. Obviously, this SSB modulation technique requires both a quadrature DDFS and a quadrature local oscillator. By using the digital frequency synthesis technique coupled with the inherent matching of monolithic CMOS analog circuits, 45 dB of SSB image rejection can be achieved without any trimming or feedback loops. Since constant-envelope FSK modulation is used and adaptive power control is required, an output programmable class-C power amplifier [11] is implemented for transmission.

In the receiver, the dehopping and down conversion process is performed in a single direct-conversion stage to save power. It would be difficult to generate accurate I-Q dehopping carriers over the 26 MHz band, using a conventional passive phase splitter. A desirable by-product of the SSB modulation technique is that if we take the imaginary part of the complex signal, as shown in (4), we get a signal which is orthogonal to the original signal obtained by taking the real part. This technique is used to generate an accurate quadrature carrier signal at RF

$$\begin{aligned} Q_{\mathrm{USB}}(t) &= \mathrm{Im}\{\exp(j2\pi f_c t)\cdot\exp(j2\pi f_x t)\} \\ &= \sin[2\pi(f_c+f_x)t]. \qquad (4) \end{aligned}$$

The receiver sensitivity is defined in decibels as [12]

$$Rx \text{ Sensitivity} = -174 \text{ dBm} + NF + \text{Noise } BW + \text{SNR} \quad (5)$$

where -174 dBm represents the thermal noise (kT) in a 1-Hz bandwidth at 300 K and NF denotes noise figure of the receiver. With 7 dB of total noise figure (including the antenna and bandpass filter loss), 80 kHz of noise bandwidth, and 10 dB of SNR

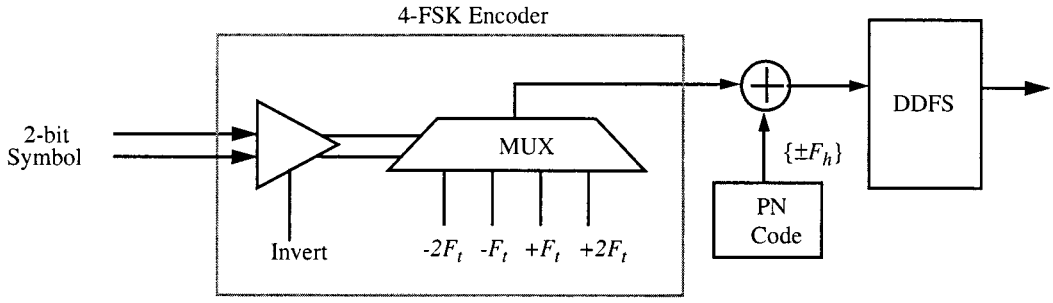


Fig. 3. Baseband transmitter block diagram (4-FSK).

threshold (in AWGN), the receiver sensitivity for our system is −108 dBm. An extra 20 dB should be added to this value if the worst case Rayleigh fading channel is considered.

B. Baseband Architecture

Low power dissipation requires that complex signal processing such as adaptive equalization be avoided if possible. Delay spread (τ_m) without countermeasures (equalization) determines the upper limit of the transmission rate through the radio channel. For outdoor microcellular channels, the value is around 0.5 μs [13]. This implies that there will be about 0.5 μs of delay dispersion due to group delay variations over different carrier frequencies. For a fast frequency-hopped system, this delay cannot be tracked by the time recovery loop. The delay spread should therefore be a fraction of the symbol time, typically one tenth or less. This suggests that the maximum transmission symbol rate possible without resorting to an expensive wideband channel equalizer is about 100 kHz. Our modulation symbol rate (80 kHz) is appropriately chosen for this requirement. Thus, no equalization is required for our receiver.

The baseband transmitter, shown in Fig. 3, is quite simple for our system, since both FSK and FH are achieved using the DDFS. Only two other blocks are required besides the DDFS/DAC combination: an encoder that translates the input symbol into an appropriate quaternary FSK frequency and a memory that stores the frequencies which correspond to the hopping patterns. These two frequencies are summed at every symbol cycle and fed into the frequency control word of the DDFS for proper tone generation. The use of the DDFS results in continuous phase changes between different frequencies, which makes the transmitted FSK signal a form of continuous-phase modulation [14]. The sidelobes of continuous-phase FSK (CPFSK) are lowered to 27 dB below the peak, compared to only 13 dB for the non-CPFSK case. Although the phase continuity of the CPM process cannot be utilized at the receiver since the channel introduces a phase jump between hops, low spectral sidelobes of the transmitter CPM spectra are still beneficial for multi-user radio scenarios.

In the receiver, automatic gain control (AGC) is required if the dynamic range of the detector is less than that encountered in the radio channel, typically 60–80 dB. Since FSK signaling only involves the frequency information, not amplitude or phase, a hard-limiter capable of more than 80 dB of dynamic range replaces an actual AGC loop. The hard-limiter works as a one-bit quantizer and makes the received signal independent of level variations. Before hard-limiting, of course, a lowpass channel filter selects the baseband signal from neighboring channels. The filter should have a wide dynamic range. Basically, a direct-conversion receiver of this nature requires that all of the building blocks, including baseband components, have a high enough dynamic range to avoid any gain control. A hard- limiter mated with a digital FSK detector was designed and evaluated for dynamic range. The measured dynamic range of the detector is 82 dB at a BER of 10^{-3} [15], which is sufficient for the radio channels encountered in most wireless applications. Due to odd harmonics produced by hard-limiting the sine waves, our approach limits the modulation scheme to binary FSK for real signal detection and to quaternary FSK for complex signal detection. However, the merits from power savings and hardware simplicity obtained from the absence of a multi-bit analog-to-digital converter (ADC) and an expensive (in both power and complexity) linear variable gain amplifier required in the AGC loop justify this architecture for a portable transceiver design.

The worst case accuracy of a crystal oscillator without complicated compensation techniques is typically ±50 ppm (parts per million). With open-loop direct conversion from a 915 MHz RF to baseband, the carrier frequency error could amount to ±100 kHz (including the transmitter error as well). The receiver therefore requires a frequency tracking loop, not for phase tracking of the carrier as in a coherent receiver, but for compensating for the frequency offset between the transmitter and receiver. A time tracking loop is also required to recover the clock from the received data. Both loops use a digital phase-locked loop (PLL) architecture with programmable loop coefficients [16]. Since our system is slow frequency-hopped, the hop rate is lower than the symbol rate, thus allowing the use of an open-loop hop time synchronization scheme in which the hop time is aligned with the symbol time plus a programmable delay to compensate for the delay between the two loops. Fig. 4 shows the proposed baseband receiver block diagram, which contains a diversity-combining FSK demodulator, and time and frequency tracking loops.

C. Implementation Imperfections

The direct-conversion architecture potentially suffers from a dc offset problem [17]. For a baseband signal of 300 μV in the direct-conversion receiver, for instance, the dc offset can be as high as a few mV, thus totally wiping out the received signal. Two main sources for this problem are mismatches in the baseband receive signal path and self-mixing of LO leakage which is

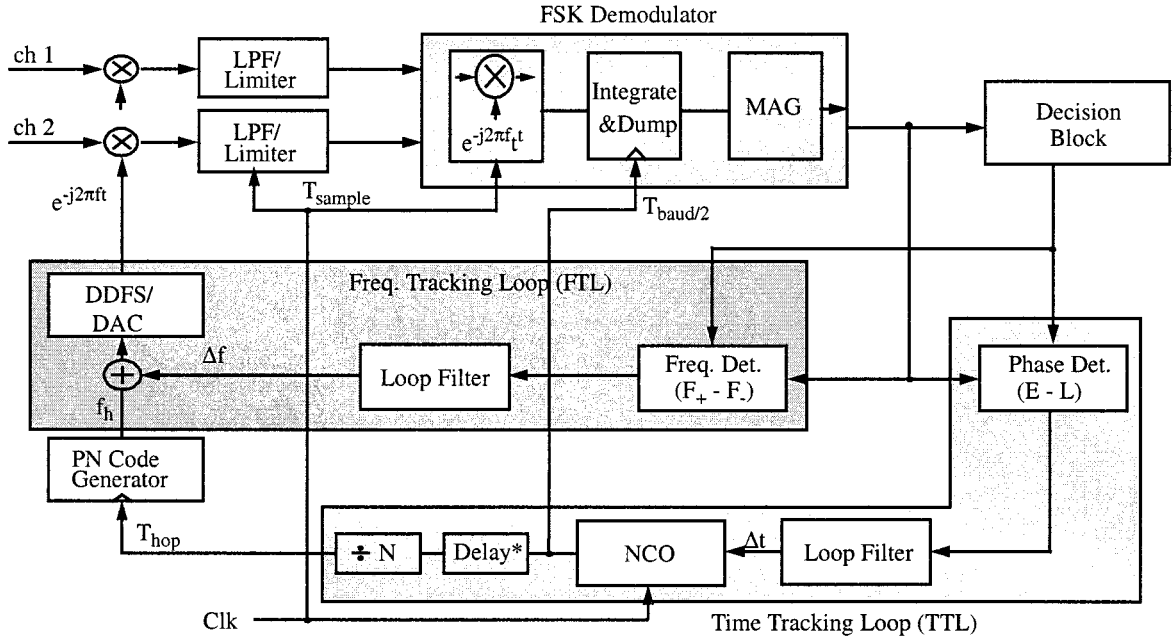


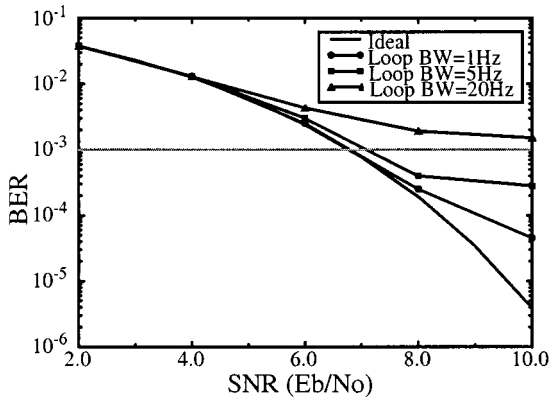
Fig. 4. Baseband receiver block diagram.

often time varying. There are several techniques to mitigate the dc offset problem. From the architecture point of view, a new type of superhet-erodyne receiver, called a "low-IF receiver" (because its IF is close to baseband), has been proposed for some GSM handsets [18]. However, this technique requires complex image suppression techniques, which are a serious bottleneck for this solution. A dc feedback loop either in the analog domain or in the mixed-signal domain using digital signal processing can also be used to mitigate this effect. For those systems with linear modulation techniques with significant energy at dc, however, this technique is very sensitive to the loop bandwidth. Fig. 5(a) shows the dc offset simulation effects over different loop bandwidths for binary PSK (BPSK) with raised-cosine filtering ($\alpha = 0.5$) at 150 kbps. If the dc offset varies faster than 5 Hz, this technique is no longer effective due to severe energy loss near dc.

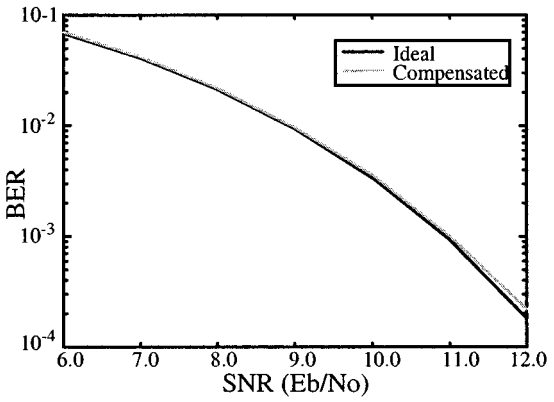
For FSK signals, which do not have any energy at dc, however, a simple ac coupling can be used. The value of ac coupling capacitance, though, may not be too large if on-chip implementation is desired. For this reason, we have adopted a dc feedback loop around the analog baseband components. Fig. 5(b) shows the effectiveness of the dc-offset compensation technique in our system. No noticeable degradation is observed, thus validating the suitability of FSK modulation for direct-conversion receivers.

A direct-conversion transceiver requires analog I-Q carrier generation. However, I-Q mismatches, both in amplitude and phase, will degrade the hardware performance. The mismatches translate into two problems. For the transmitter, the SSB technique deviates from the ideal case, thus producing an unwanted image signal. The effect of degradation is captured in the following equation [19]:

$$\frac{P_{\text{spur}}}{P_{\text{desired}}} = \frac{1+\gamma^2-2\gamma\cos\phi}{1+\gamma^2+2\gamma\cos\phi} \tag{6}$$



(a)



(b)

Fig. 5. BER versus SNR due to dc offset compensation. (a) BPSK (dc feedback). (b) BFSK.

where γ is the gain ratio of the I-Q branches (I/Q) and ϕ is the phase error (the deviation from $\pi/2$). For instance, with a 3-degree phase mismatch and a 3% amplitude deviation, the maximum achievable SSB suppression is only 35 dB. For the

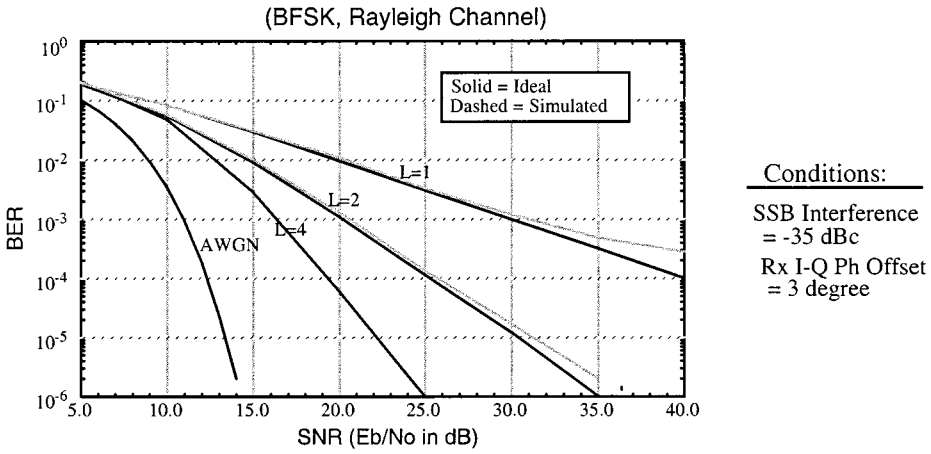


Fig. 6. I-Q mismatch simulation.

receiver, the I-Q mismatches affect the orthogonality property of I-Q signal pairs. A monolithic design with careful transistor matching, though, can guarantee reasonable I-Q matches: typically, a phase mismatch of 1 degree and a gain imbalance of 2%. If further accuracy is required, the designer must resort to other advanced techniques such as device trimming and some type of gain and feedback loop.

The combined effects of I-Q mismatches have been simulated for our transceiver (Fig. 6). The unwanted SSB image of a transmitter is modeled as a cochannel interference to another user. Simulation results have shown that there is little degradation, as long as the SSB image is suppressed more than 35 dB below the desired signal. The issue of sensitivity to mismatches was also studied via simulation (Fig. 7). The received signal is relatively insensitive to mismatches: the amplitude mismatch is unimportant due to hard-limiting, and the phase mismatch is less critical since the orthogonal FSK signals are detected noncoherently. Since our system is more sensitive to the transmitter I-Q mismatches than the receiver mismatches, the more strict requirement of a 45-dB SSB image suppression is specified for the transmitter.

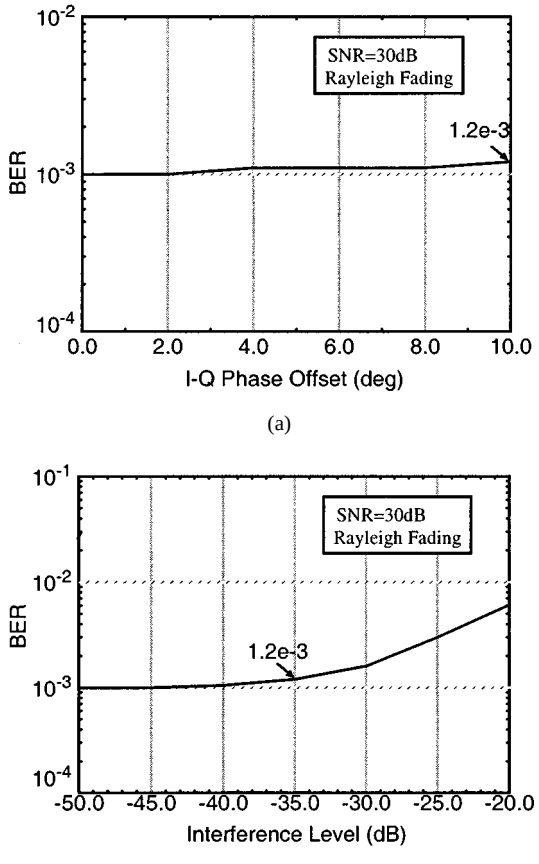


Fig. 7. Performance sensitivity to mismatches. (a) Sensitivity to Rx I-Q phase mismatch. (b) Sensitivity to SSB interference.

IV. Detailed Baseband Processing Blocks

A. Channel-Select Filter

For a direct-conversion receiver, channel selection is performed at baseband using a lowpass filter. Given the quaternary frequency tone assignment (Fig. 1 of Section II), the passband corner frequency of the lowpass filter is chosen to be 230 kHz (with passband ripple <1 dB), and the stopband frequency ($F_{\rm stop}$) is 320 kHz. $F_{\rm stop}$ actually corresponds to a tone from the adjacent user; therefore, a minimum of 50 dB rejection is required. This guarantees 24 dB of rejection at the 6-dB signal bandwidth of the unwanted tone. The noise bandwidth of the entire analog system is set by the passband of the channel-select filter (230 kHz). The passband frequency is chosen such that there is no significant energy loss for desired signals, and the group delay whose peak occurs at the corner frequency is relatively small over the frequency range of interest. The latter condition limits the variation of the group delay over the signal bandwidth. The sharp transition of this channel filter requires a relatively high-Q design. Therefore, a sixth-order elliptic filter is required and switched-capacitor techniques have been adopted for its implementation.

When an FSK signal passes though a band-limiting filter, the signal gets distorted both in amplitude and zero-crossing locations. When this happens at baseband with a highly selective lowpass filter, the distortion becomes even worse since there are only one or two cycles per symbol. There are two main sources

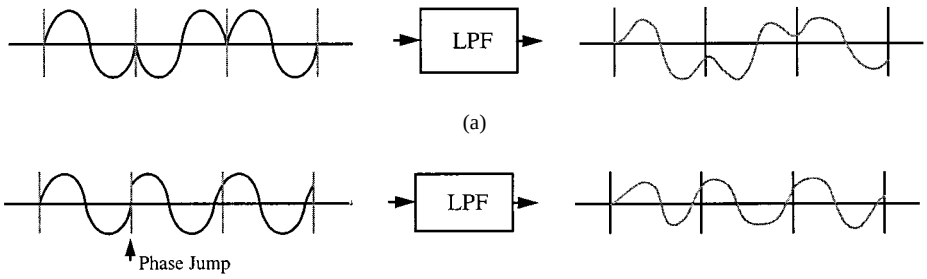


Fig. 8. Channel filter distortions. (a) At data transitions (between $+F$ and $-F$. (b) At hop boundaries.

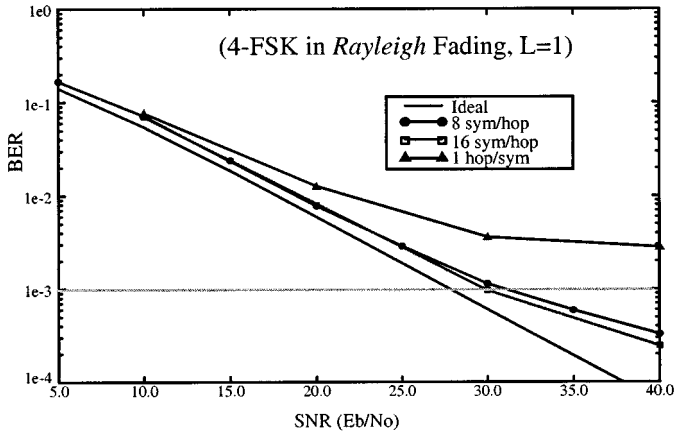


Fig. 9. Hop rate simulation.

for these transient filter distortions. First, the lowpass filter distorts the signals at data transitions, as shown in Fig. 8(a), since there are 180 degree phase changes when data is alternating between 1 and 0. This is inherent in any direct-conversion receiver using a complex detection scheme because of unavoidable phase jumps between positive and negative frequencies. For a frequency-hopped system, phase discontinuity is also experienced at hop boundaries as shown in Fig. 8(b). An FH system should guarantee independent fades in each hop, which is required for diversity combining and channel decoding. For a fast FH system, this is achieved by hopping to many different frequencies for each symbol; however, the transient filter distortion problem becomes worse by doing so. Slow FH with interleaving alleviates this problem while maintaining independent fading between symbols when properly deinterleaved at the receiver (mainly because phase jumps between hops occur much less frequently). Simulation results have shown that slow FH significantly reduces the overall channel filter distortion effects (Fig. 9). In order to balance the performance improvement with the interleaver complexity and processing delay penalty, a rate of 8 symbols per hop was chosen as the baseline hop rate. A convolutional interleaver/deinterleaver whose size is 8×40 guarantees that symbols with the same hop frequency are separated by at least 40 symbol durations, which is required for the proposed rate-1/2 Viterbi decoder [20]. The overall delay of our interleaving and deinterleaving block is 280 symbols, which corresponds to 3.5 ms for $T_{\text{baud}} = 12.5\ \mu$s (80 kHz).

B. FSK Detector

It is well known that the optimum FSK detector is a correlation detector. The following correlation value (CV) is evaluated for each tone:

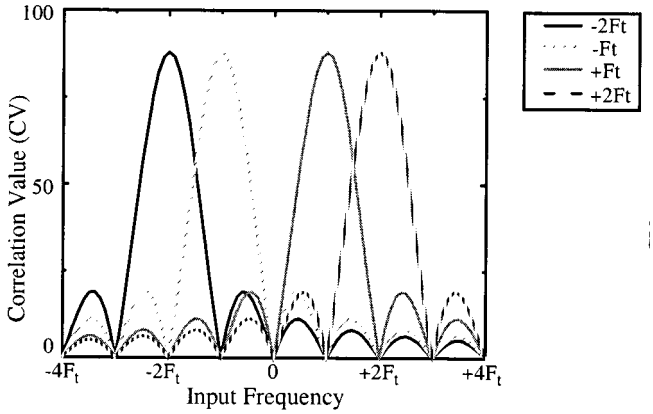
$$CV(f_t) = \left| \frac{1}{N} \sum_{n=0}^{N-1} \tilde{s}(nT_s)\{\cos(2\pi f_t nT_s) + j \sin(2\pi f_t nT_s)\} \right| \tag{7}$$

where

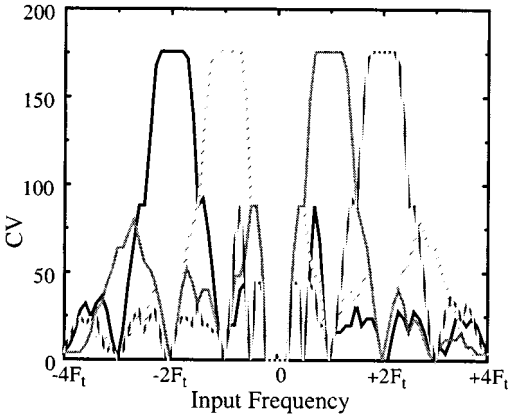
$\tilde{s}(nT_s)$	quadrature input signal;
f_t	tone frequency to be detected;
T_s	sampling clock period;
N	oversampling ratio (T_{baud}/T_s).

This is in some sense equivalent to a Discrete Fourier Transform technique, where a particular tone frequency is downconverted to dc, filtered by an integrate-and-dump (I&D) block, and its energy is detected. The magnitudes of the tone energies are compared, and the tone with the maximum correlation value is chosen as the transmitted tone.

However, this detector is not often used in practice owing to the complexity of the required circuits. A simple version of a digital FSK correlation detector has been designed for use in a frequency-hopped direct-conversion receiver. An exclusive-NOR gate is used as a one-bit multiplier for signal correlation with the hard-limited baseband signal. However, the orthogonality of FSK tones may be corrupted due to harmonic aliasing [21] unless the oversampling ratio N is chosen properly to guarantee that the generated harmonics are symmetric about half of the sampling frequency, retaining the Hermitian property of each I-Q signal. An integer multiple of eight ($8i$) for quaternary FSK and an integer multiple of four ($4i$) for binary FSK meet this requirement (Fig. 10). Though it does not exactly mimic the ideal frequency discrimination plot, the curve for our detector still displays nulls at the desired tone frequencies. The quaternary detector must then only discriminate between signal energy at the tone frequencies of the set $\{+2F_{\text{tone}}, +F_{\text{tone}}, -F_{\text{tone}}, -2F_{\text{tone}}\}$. For the magnitude calculation unit, an absolute-value addition block replaces a conventional squaring multiplier followed by a summing node. Thus, a truly multiplierless FSK detector is obtained with little performance degradation. Simulation results show about 1.2 dB of implementation loss for our detector from the ideal detector. This degradation is mainly due to the transient filter distortions aforementioned.



(a)



(b)

Fig. 10. Frequency discrimination the FSK detector ($N = 88$). (a) Ideal correlation. (b) 1-bit correlation.

The architecture of the overall quaternary FSK demodulator is shown in Fig. 11. It uses three such quadrature correlators: two for the two tone pairs and a third for $\pm F_{\text{tone}}/2$, which is used as the frequency error detector for the frequency tracking loop. The I-Q local tone generator is implemented with a one-bit output numerically-controlled oscillator (NCO). The reference tone frequency to be detected is fully programmable by controlling the input control word of the quadrature NCO. The proposed transceiver can handle various data rates between 2–160 kbps. When the (coded) data rate is lower than the fixed modulation rate of 80 kBaud for quaternary FSK, the data may be repeated in symbol format. The repeat code provides extra diversity over a Rayleigh fading channel when independent hops of the same information are combined after deinterleaving. Compared to antenna diversity which can be thought of as a parallel diversity scheme, hop combining can be interpreted as a *sequential* diversity scheme. It should be noted that for a quaternary FSK system with FH, symbol deinterleaving requires all four correlation values to be processed through both the deinterleaver and hop combiner before making decisions for the channel decoder input.

V. Synchronization Issues

The synchronization scheme, both acquisition and tracking, is based on a simple time division duplexing frame structure, which consists of a pilot tone, a frame ID (*Word Sync*), and actual data [22]. The acquisition process is accomplished by means of frame synchronization, based on coarse energy detection of the received signal and the pattern matching of a 21-digit Barker code. The proposed wake-up tone scheme for synchronous-access frequency-hopped transceivers is much simpler than a parallel search method based on parallel matched filters and relatively faster compared to a PN acquisition scheme based on serial search [23].

A. Frame Structure

A simple frame structure with TDD has been developed for transmitter and receiver synchronization, as shown in Fig. 12. The frame structure consists of a pilot tone (C0), a unique word (C1), and actual data (C2). The C0 and C1 fields are for control slots and used in the acquisition process: C0 for energy detection and C1 for pattern matching. Their carrier frequency can be either fixed to a predefined acquisition frequency or hopped to a limited number of known frequencies. The acquisition time is shorter if the acquisition frequency is fixed since there is no need for sequential search. However, if the preassigned acquisition frequency receives interference or jamming for some unexpected reasons, a set of frequencies (even two) would be helpful to initiate a robust acquisition link. The carrier will of course be hopping during the C2 slots, where time and frequency are tracked. Although the baseline modulation scheme is quaternary FSK, only binary tones will be sent during the control slots (C0 and C1) to make acquisition easier. A dead zone (D) is inserted between the transmit and receive frames to account for the processing delay of the transceiver and the average propagation delay of the radio channel.

A typical frame length proposed for digital wireless systems ranges from 2 to 20 ms. The choice of the frame length trades off the overall link delay with the channel bandwidth efficiency. Since an overall transmission delay of 20–40 ms is acceptable for voice communication, a total frame length of 20 ms, 10 ms each for the transmit subframe and the receive subframe, is chosen. The combination of C0, C1, and D slots compose 20% of the total frame slots. Thus, an 80% channel utilization can be achieved.

B. Acquisition

Acquisition in time, frequency, and hopping code is accomplished by means of frame synchronization. The control flow of this process is shown in Fig. 13. It is achieved in two steps: coarse acquisition (energy detection) and fine acquisition (pattern matching of the frame ID).

Coarse Acquisition: A purely digital receiver signal strength Indicator (RSSI) detection scheme using both energy detection and relative slope detection cannot be utilized since the hard-limiter eliminates absolute energy detection capability in the digital domain. Moreover, the required, digital matched filter has a sinc-shaped frequency spectrum associated with it. If the frequency offset pushes the tone frequency to the null locations, this scheme has no way of distinguishing the pilot tone. Therefore, the analog RSSI-aided energy detection scheme is used instead. In this scheme, the RSSI output, which is generated by a cascade of logarithmic amplifiers after the channel-select filter, is used

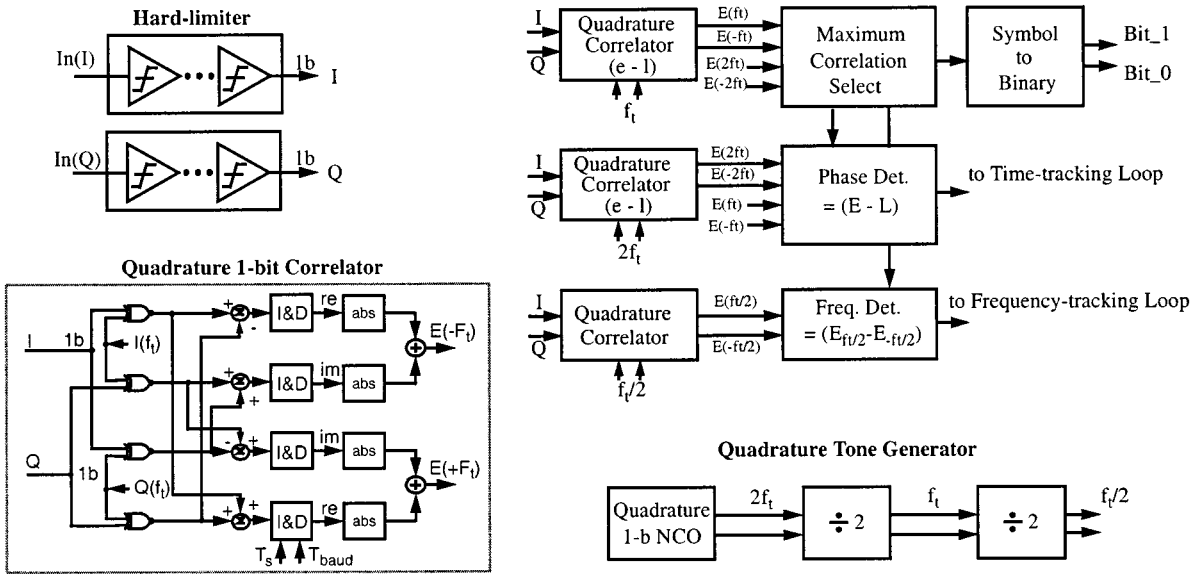


Fig. 11. Multiplierless quaternary FSK detector.

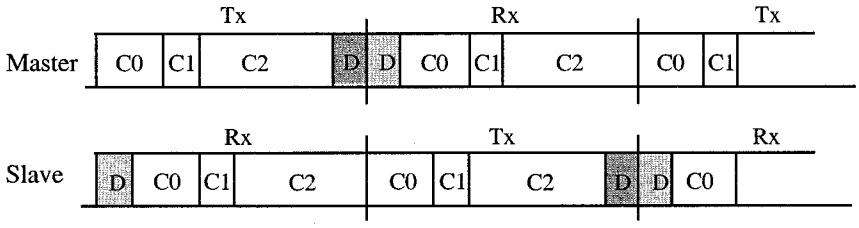


Fig. 12. TDD frame structure.

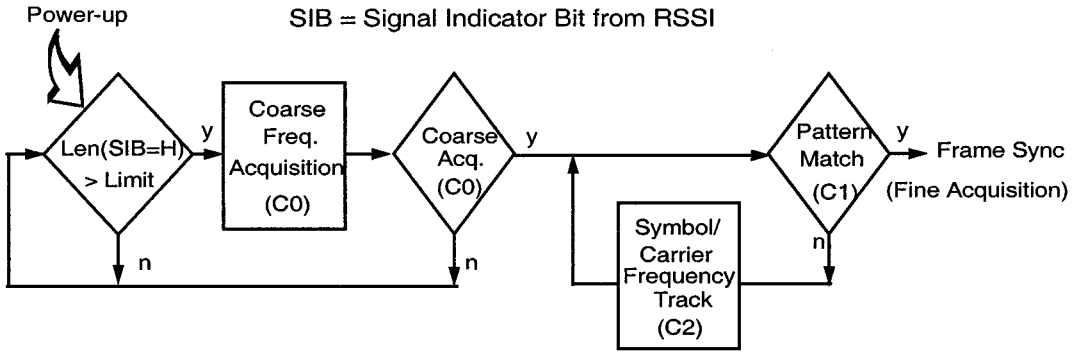


Fig. 13. Frame synchronization control flow.

to coarsely indicate whether the C0 pilot tone is present or not. The slave handset first listens for the pilot tone of the frame (C0) which is broadcast by the master on a preassigned acquisition carrier frequency. The RSSI output is then compared to a programmable energy threshold value to produce either high or low output (Fig. 14). This signal indicator bit (SIB) indicates whether a signal is present at a particular acquisition frequency or not. The energy threshold voltage is generated by an 8-bit digitally controlled sigma–delta DAC. In theory, the threshold value can just be slightly above the noise level, since there is another level of security checked by the pattern matching logic. However, it should be set sufficiently high enough to optimize the total acquisition time by reducing the probability of false alarms.

Once the SIB goes high, frequency acquisition takes place by sweeping the frequency of the DDFS with a step size of $F_{\text{tone}}/4$ (20 kHz). The frequency sweeping is required since the worst possible frequency error ($\pm$100 kHz) may be more than what the frequency tracking loop can handle. The 5-bit correlation value of a predetermined tone ($+F_{\text{tone}}$) is evaluated to indicate a coarse frequency lock. After coarse frequency acquisition, the rest of the C0 slots are used to detect a signal transition from $+F_{\text{tone}}$ to $-F_{\text{tone}}$. The timing acquired during the C0 slots still has a $\pm T_{\text{baud}}$ uncertainty associated with it since symbol synchronization has not been yet achieved. Therefore, the received data needs to be matched with the unique word pattern before frame synchronization is declared. Once *frame sync* is declared, the receiver

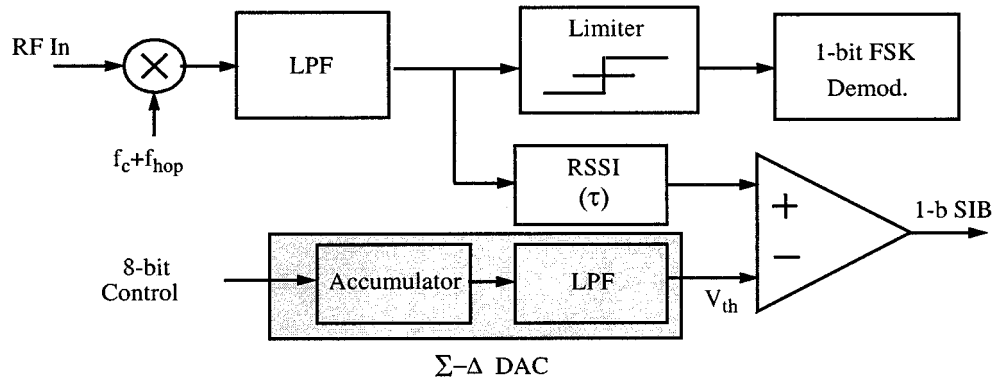


Fig. 14. Signal indicator bit (SIB) generator.

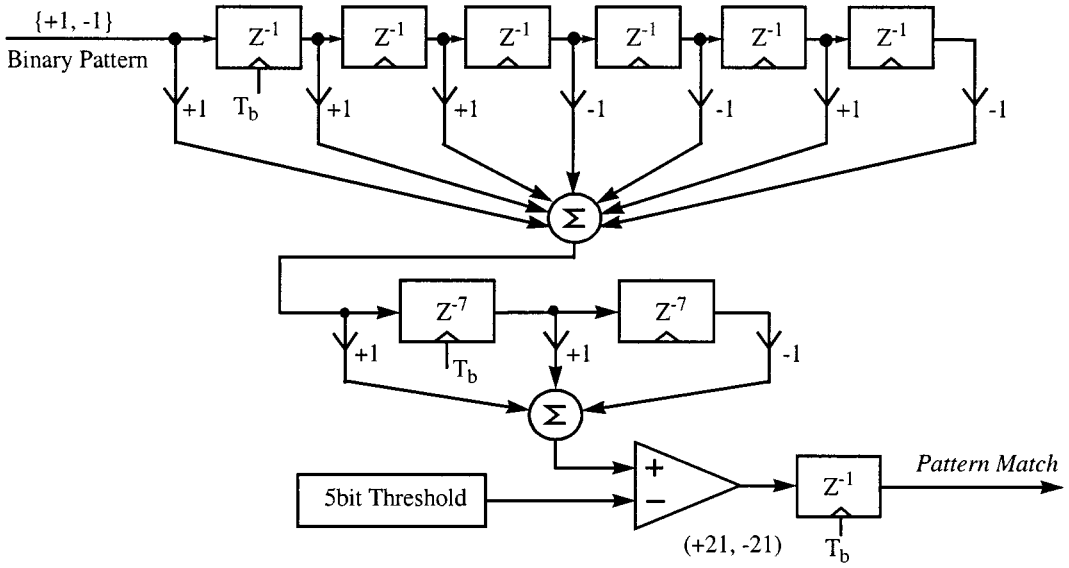


Fig. 15. C1 pattern recognizer.

starts demodulating data. The hopping code synchronization relies on the fact that once the frame is synchronized, a predefined frequency hopping pattern is repeated every frame. Thus, no extra pseudonoise (PN) code acquisition is required as in a DS system.

C1 Pattern Recognizer: Pattern matching of the C1 code is required for frame synchronization. A 21-digit binary Barker code [24] is used for this purpose. Rather than having 21 independent digits, the pattern consists of three subsets of a seven-digit code $\{1\,1\,1\,-1\,-1\,1\,-1\}$: the first two sets have a positive polarity and the third one has a negative polarity. This way, the number of fan-ins to the summing adder can be substantially reduced. The maximum correlation value is $+21$; therefore, a 5-bit programmable threshold value is sufficient. The block diagram of the C1 pattern recognizer is shown in Fig. 15. Simulation results have shown that a threshold of 16, which allows two random errors in the pattern, is a reasonable choice to declare a pattern match (Fig. 16). Even with 15 dB of SNR, this threshold was able to discriminate the pattern from noise. The peak correlation value was 17 while the next highest value near the symbol digit (within ± 4 symbol durations) was only 3 with the following conditions: timing phase error $(T_{\rm err}) = T_{\rm baud}/4$ and frequency error $(F_{\rm err}) = F_{\rm baud}/8$ (10 kHz). Alternatively, a threshold of 18 can be used if a tighter acquisition condition (for example, $T_{\rm err} = T_{\rm baud}/8$ and $F_{\rm err} = F_{\rm tone}/16$) is required. Since a coarse acquisition is achieved by detecting the signal transition at a predefined location in the C0 field, the pattern matching process can only be enabled over a certain window period, for example plus or minus four symbol cycles around the expected time instant. This makes the fine acquisition process more robust and a 21-digit pattern sufficient for our purpose.

C. Tracking

The acquisition process only guarantees the accuracy of the symbol clock and carrier frequency to within a reasonable range of error. It is thus up to the time and frequency tracking loops to pull in the remaining errors and maintain lock. A tracking loop requires phase-locked loop (PLL) techniques whose implementation can be completely analog, digital, or a combination of both. Since a DDFS is used for hopping carrier generation and the symbol clock frequency is relatively low (80 kHz) in the FH/SS transceiver, both the time and frequency tracking loops have adopted a fully digital-PLL architecture, as shown in Fig. 4 of Section III.

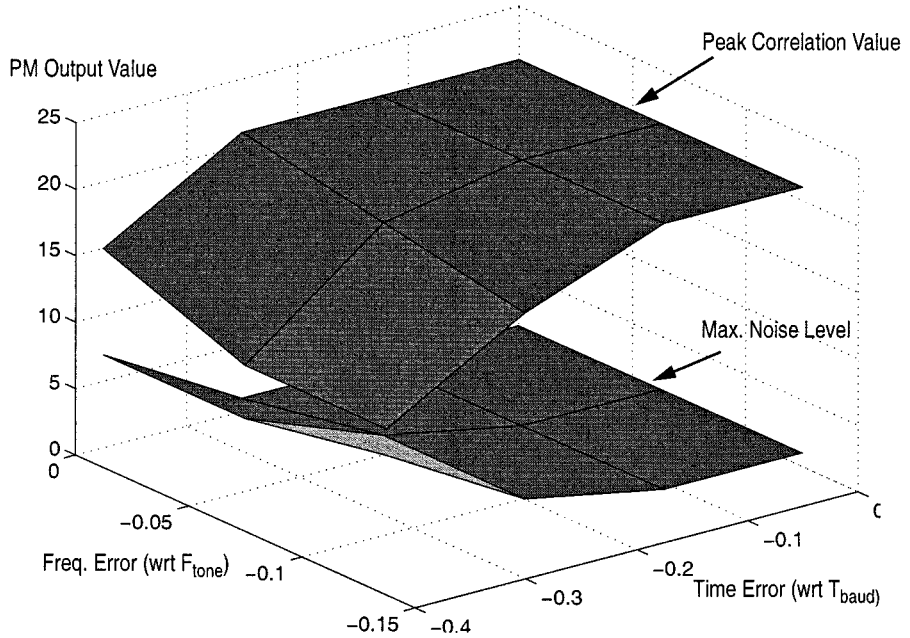


Fig. 16. Pattern matching simulation.

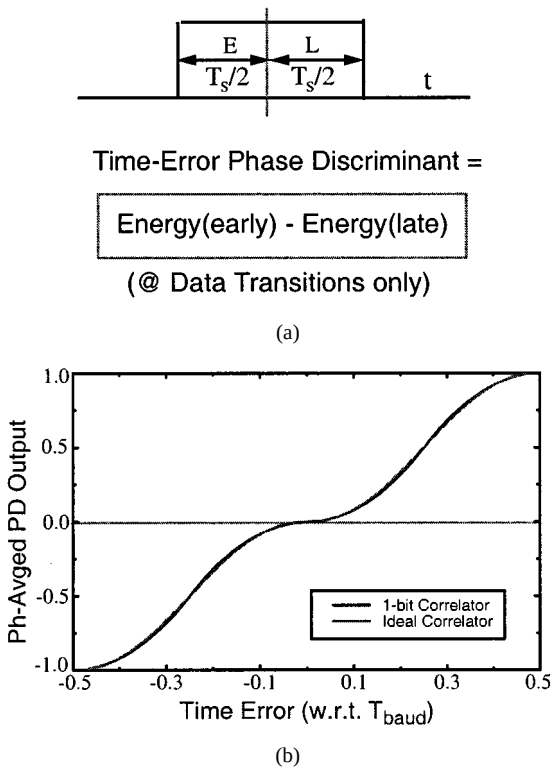


Fig. 17. Phase error detection of TTL. (a) Detection algorithm. (b) S-curve.

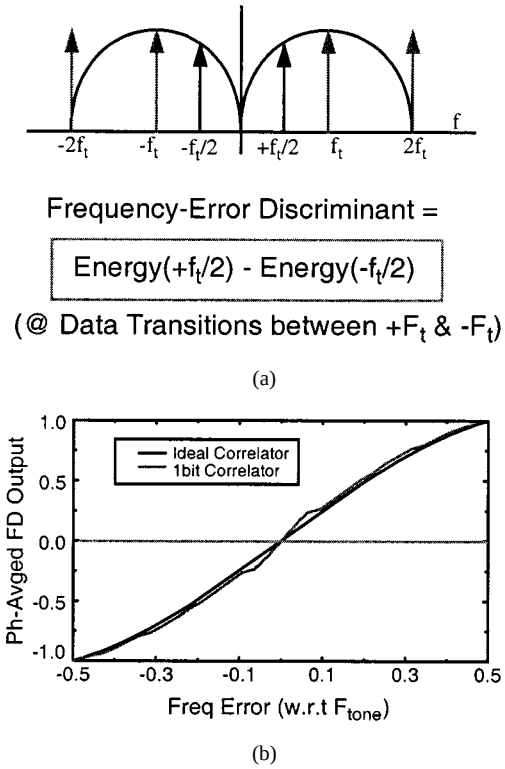


Fig. 18. Frequency error detection of FTL. (a) Detection algorithm. (b) S-curve.

The time tracking loop (TTL) consists of a phase detector (PD), a loop filter, and an NCO. An early-late phase detection scheme is used to generate a phase discriminant. The FSK demodulator uses only one-bit signal correlation. As shown in Fig. 17(b), though, the shape of the 1-bit correlator S-curve closely resembles that of the ideal case when the PD output is averaged over different carrier phases. The correlation energy of the first-half symbol minus that of the second-half symbol is detected for each tone [Fig. 17(a)] and the output from one of the four tones, chosen by the hard decision bits, is fed into the loop filter.

When the frequency offset is relatively large, as in this FH system, a frequency-locked loop (FLL) is required rather than a PLL. The digital FLL consists of a frequency detector (FD), a loop filter, and a DDFS. The maximum frequency error it can correct is now limited by the S-curve characteristics of the frequency detector [Fig. 18(b)], typically up to half of the symbol rate. The DDFS in this case just maps the input frequency to

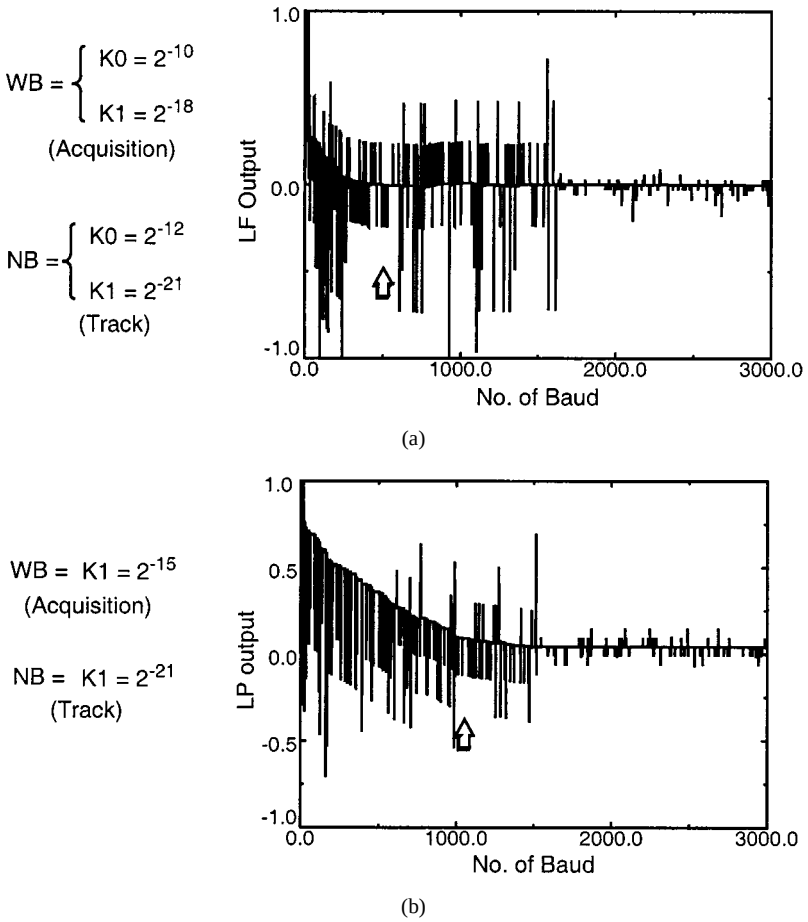


Fig. 19. Loop simulation example. (a) TTL loop filter output trajectory. (b) FTL loop filter output trajectory.

the output frequency with a linear gain. The overall loop is thus first-order.

The difference between the two correlation energies at frequency nulls of the $+F_{\rm tone}$ and $-F_{\rm tone}$ data can be used as the FD output; however, this provides a lower over-all loop gain. Thus, it is not selected. Instead, the difference between the two correlation energies at $+F_{\rm tone}/2$ and $-F_{\rm tone}/2$ is used as the baseline frequency discriminator [Fig. 18(a)]. When a signal with either $+F_{\rm tone}$ or $-F_{\rm tone}$ is received, its correlation value is stored and compared with the other correlation value. The FD output is then fed into the loop filter only when a transition from $+F_{\rm tone}$ to $-F_{\rm tone}$ or vice versa occurs. Statistically speaking, the loop is activated only in one out of eight clocks due to the data transition restriction in our FD scheme, thus slowing down the frequency tracking process. To speed up the tracking process, the difference between two correlation values at $+3F_{\rm tone}/2$ and $-3F_{\rm tone}/2$ can also be used; however, this scheme requires more complex circuits, especially since the $3F_{\rm tone}/2$ tone cannot be generated by simple binary division from the $2F_{\rm tone}$ reference tone. Thus, it is not utilized.

Fig. 19(a) shows an example of TTL simulations. The loop filter output trajectory is shown as the number of symbol intervals increases for a worst case condition with a phase error of 180 degrees and a clock frequency error of 250 Hz ($\sim$3000 ppm with respect to $F_{sym} = 80$ kHz). Two different sets of coefficients are used for acquisition: an initial wide loop bandwidth and a narrow loop bandwidth for final tracking. A steady-state condition (or lock) is accomplished in about 500 symbol cycles and the loop is switched to a tracking mode at about the 1600th symbol cycle. Fig. 19(b) shows a simulation example with a frequency error of 20 kHz ($F_{\rm tone}/4$). Acquisition is achieved in about 1000 symbol cycles.

VI. Conclusion

In this paper we have examined the system rationale, hardware architecture, and synchronization issues of a frequency-hopped transceiver for wireless personal communications. Robust operation of the transceiver is achieved through the use of space diversity (dual antennas with equal gain combing), frequency diversity (spread spectrum), and time diversity (sequential hop combining and channel coding with interleaving). The proposed transceiver employs such architectural techniques as digital hopping frequency synthesis, direct conversion, SSB modulation, hard-limiting, and multiplierless quaternary FSK detection. The digital frequency synthesis technique enables the fast hopping required for an FH-CDMA system. The TDD scheme allows one hopping synthesizer to be shared between transmit and receive modes. The hop rate has been chosen to minimize the channel filter's transient distortions. The dc-offset problem frequently encountered in direct-conversion transceivers can easily be dealt in an FSK system without resorting

to expensive signal processing. The SSB modulation technique eliminates often difficult-to-implement image-reject filters for signal upconversion. A baseband multiplierless correlation detector has been proposed to simplify quaternary FSK detection without automatic gain control at RF. These techniques combined allow a highly integrated monolithic solution of the entire FH/SS transceiver, thus achieving the low power and low complexity required for a handheld communications device without sacrificing robustness.

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