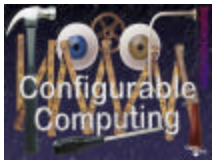
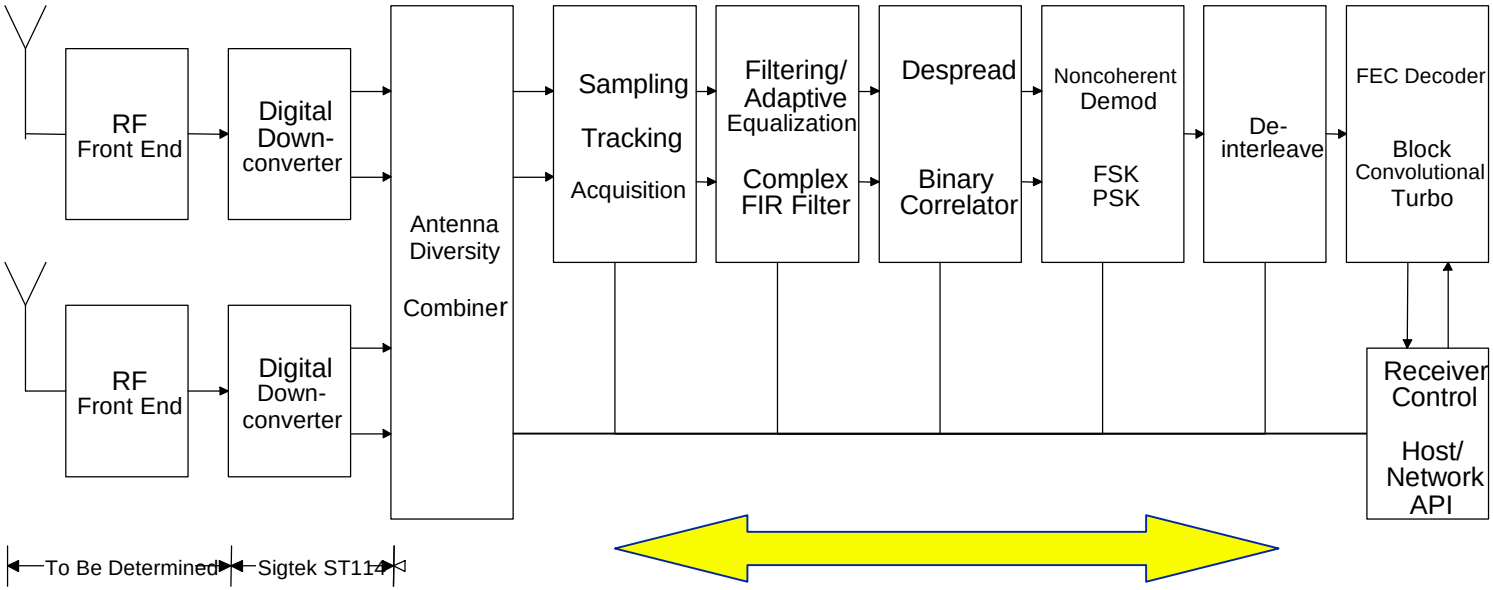


Architecture for a General Purpose Configurable Radio

Phase 1 Implementation of the Configurable Radio



Direction for replacement of DSP µP functions with reconfigurable computing

Reconfigurable Computing Modules Under Development

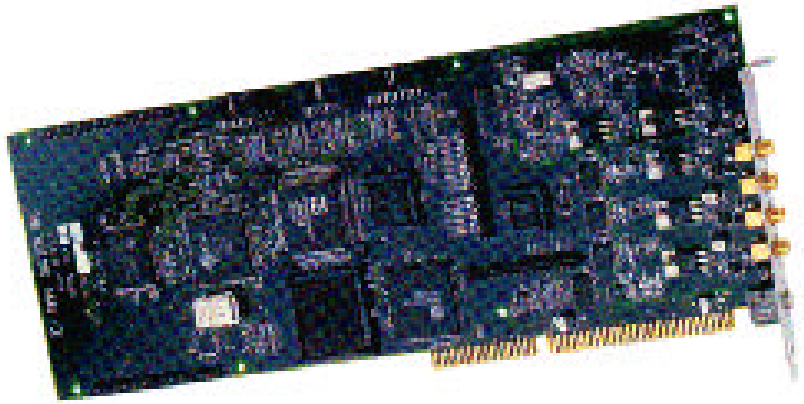
- Turbo Coder/Decoder
- Equalizer/ Single User CDMA Receiver
- Symbol/Carrier/Code Synchronizers
- Next Modules
  - → Generic sample rate converter
  - → Coder/Decoder library
  - → Demodulator library

RF Front End

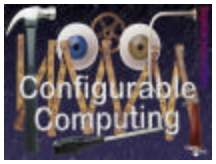
Analog Tuner:

→Downconverts from an RF of 2050 MHz to an IF of 68 MHz for bandpass digitization

→RF and IF filtering used to reje frequencies

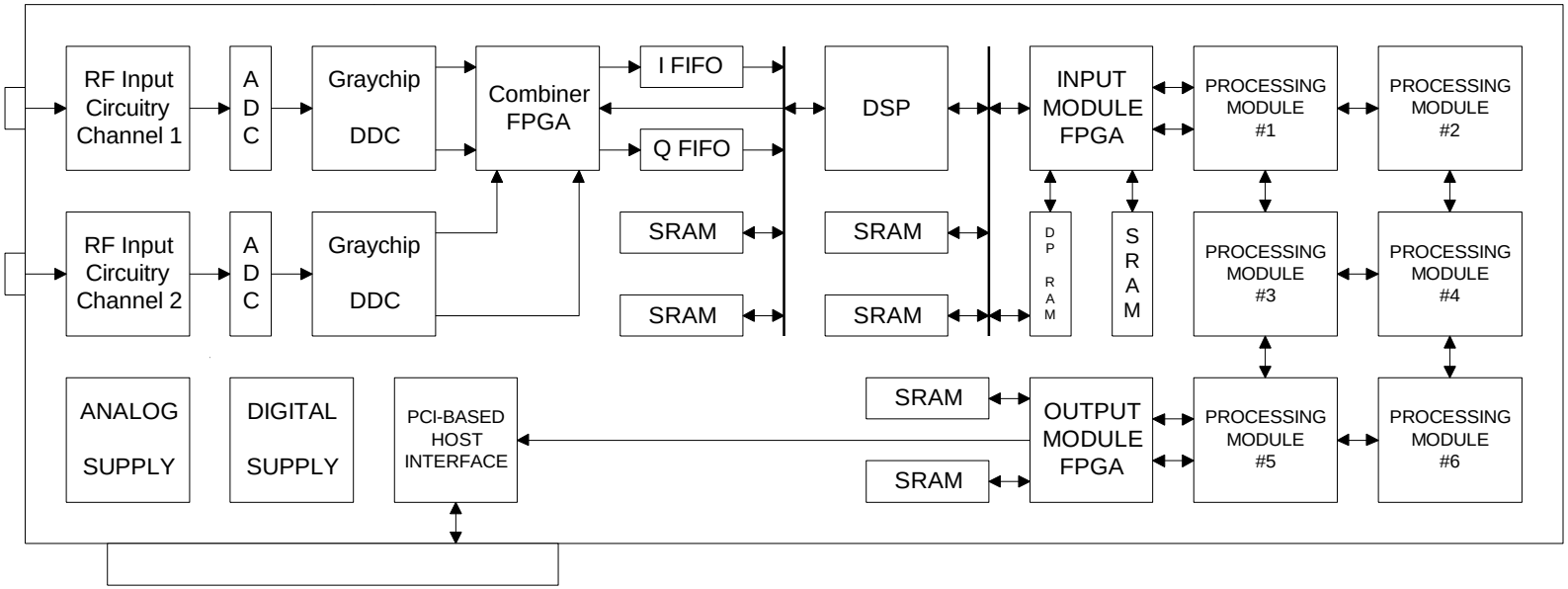


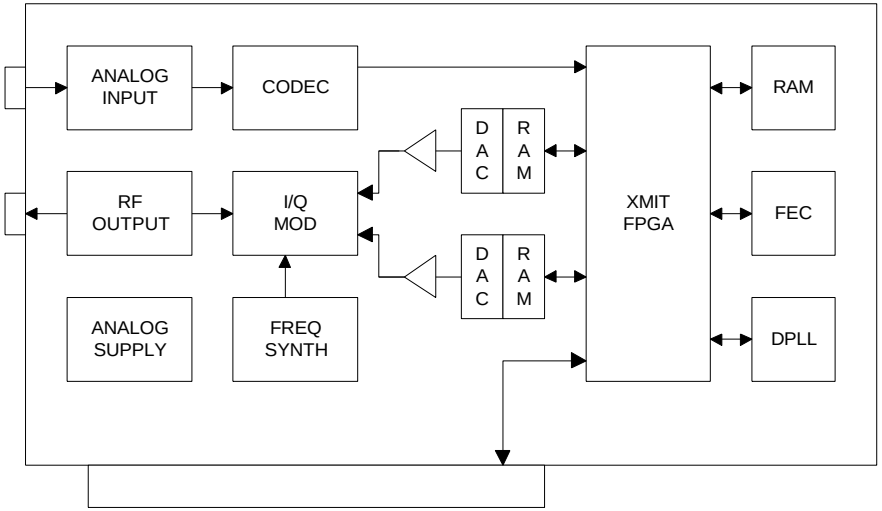
- ST-114 Digital Down-converter:
  - →HSP 50214 processor
  - →Combines quadrature mixing to complex baseband, digital filtering and decimation
  - →Up to 1.2 MHz of bandwidth
- Custom RF and IF analog filters
- Later Stages - Migrate to custom digital down-converter front end



Evolution of the Configurable Computing Platform and Configurable Radio

Phase 3 Final Architecture



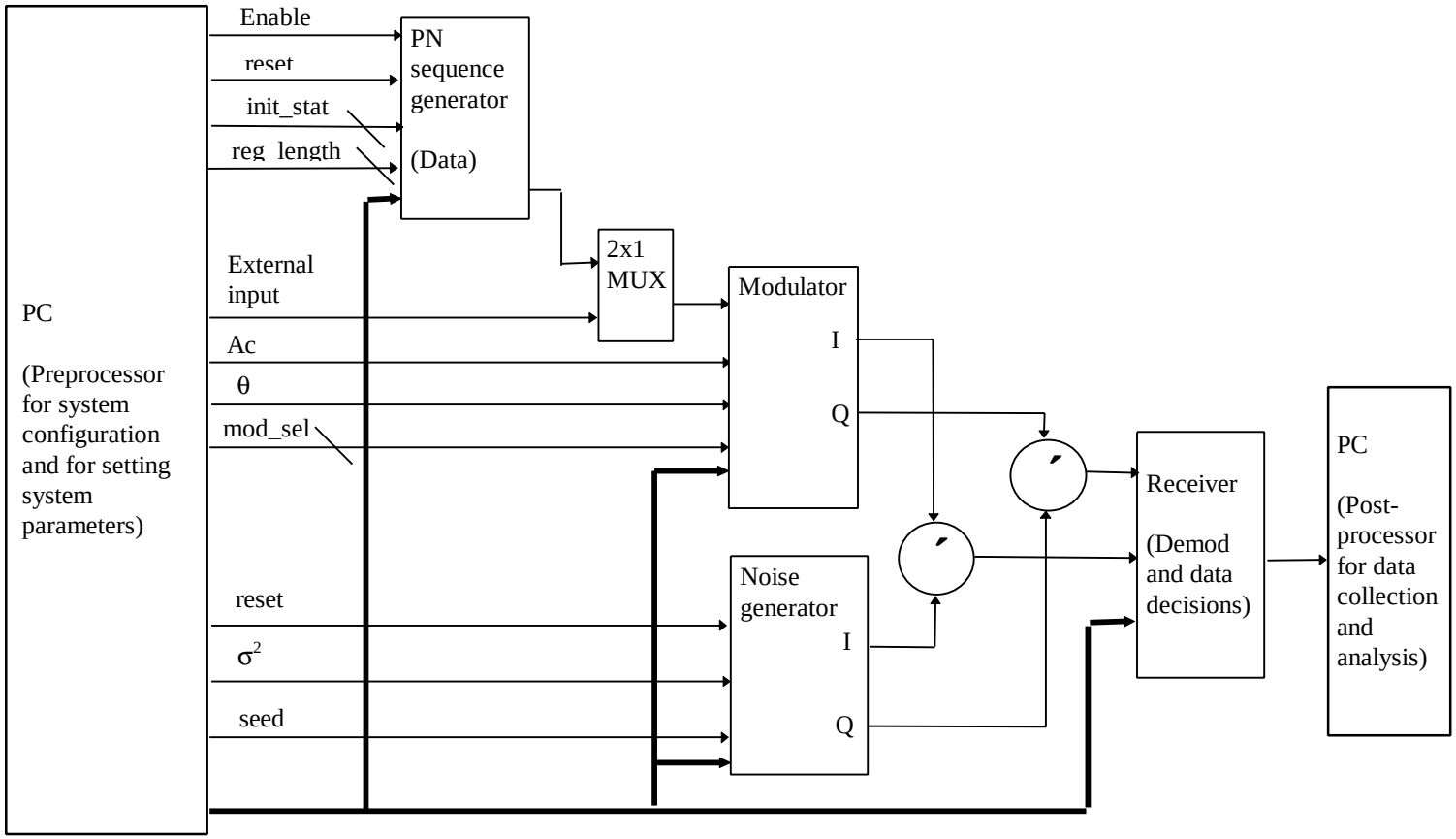


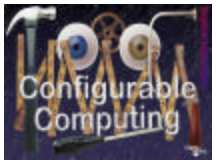
Features

- Wider bandwidth front end
- Stallion processor
- Run-time reconfiguration
- Library of communication functions

Hardware Based Simulator

- Fast simulation engine by taking advantage of reconfigurable processor
- Supports radio development effort





Summary

- Architecture of flexible high-performance radio test-bed outlined
- Stream-based approach increases flexibility of pipeline architecture
- Configurable computing very promising to modern and future communication systems